CDB42448

Evaluation Board For CS42448

Features

- Single-ended/Single-ended to Differential Analog Inputs
- Single-ended/Differential to Single-ended Analog Outputs
- CS8406 S/PDIF Digital Audio Transmitter
- CS8416 S/PDIF Digital Audio Receiver
- Header for Optional External Software Configuration of CS42448
- Header for External DSP Serial Audio I/O
- 3.3 V Logic Interface
- Pre-defined Software Scripts
- S/PDIF-to-TDM Conversion for Easy Evaluation of the TDM Digital Interface
- Demonstrates Recommended Layout and Grounding Arrangements
- Windows® Compatible Software Interface to Configure CS42448 and Inter-board Connections

ORDERING INFORMATION

CDB42448 Evaluation Board

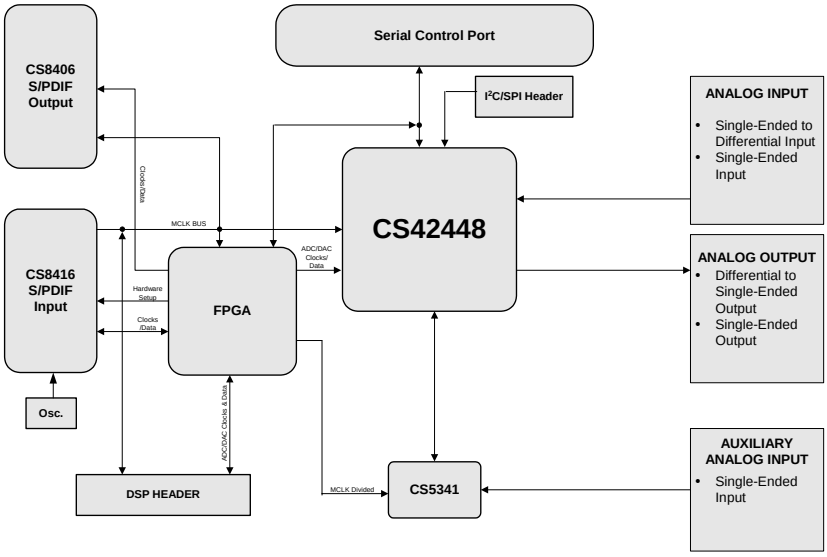
Description

The CDB42448 evaluation board is an excellent means for evaluating the CS42448 CODEC. Evaluation requires an analog/digital signal source and analyzer, and power supplies. A Windows® PC compatible computer must be used to evaluate the CS42448.

System timing for the I²S, Left-Justified and Right-Justified interface formats can be provided by the CS42448, by the CS8416, or by a DSP I/O stake header with a DSP connected. System timing for TDM mode is provided by an FPGA using clocks derived from the CS8416 or DSP I/O header.

RCA phono jacks are provided for the CS42448 analog inputs and outputs. Digital data I/O is available via RCA phono or optical connectors to the CS8416 and CS8406.

The Windows® software provides a GUI to make configuration of the CDB42448 easy. The software communicates through the PC's serial port to configure the control port registers so that all features of the CS42448 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.



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1. SYSTEM OVERVIEW

The CDB42448 evaluation board is an excellent means for evaluating the CS42448 CODEC. Analog and digital audio signal interfaces are provided, an FPGA used for easily configuring the board and a 9-pin serial cable for use with the supplied Windows® configuration software.

The CDB42448 schematic set has been partitioned into 10 pages and is shown in Figures 9 through 18.

1.1 Power

Power must be supplied to the evaluation board through the +5.0 V, +12.0 V and -12.0 V binding posts. Jumper J1 connects the VA supply to a fixed +5.0 V or +3.3 V supply. VD, VLS and VLC are all hard-tied to +3.3 V. All voltage inputs must be referenced to the single black binding post ground connector (Figure 18 on page 40).

WARNING: Please refer to the CS42448 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS42448 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 9 on page 31 provides an overview of the connections to the CS42448. Figure 19 on page 41 shows the component placement. Figure 20 on page 42 shows the top layout. Figure 21 on page 43 shows the bottom layout. The decoupling capacitors are located as close to the CS42448 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 FPGA

See “FPGA System Overview” on page 9 for a complete description of how the FPGA (Figure 10 on page 32) is used on the CDB42448.

1.4 CS42448 Audio CODEC

A complete description of the CS42448 (Figure 9 on page 31) is included in the CS42448 product data sheet.

The required configuration settings of the CS42448 are made in its control port registers, accessible through the “CS42448” tab of the Cirrus Logic FlexGUI software.

Clock and data source selections are made in the control port of the FPGA, accessible through the “FPGA” tab of the Cirrus Logic FlexGUI software. Refer to registers “CODEC SDINx Control (address 02h)” on page 17 and “CODEC Clock Control (address 03h)” on page 18 for configuration settings.

1.5 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter (Figure 11 on page 33) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS42448 to the standard S/PDIF data stream. The CS8406 operates in slave mode, accepting either a 128Fs or 256Fs master

clock on the OMCK input pin, and can operate in either the Left-Justified or I²S interface format.

Selections are made in the control port of the FPGA, accessible through the “FPGA” tab of the Cirrus Logic FlexGUI software. Refer to register “CS8406 Control (address 04h)” on page 19 for configuration settings.

1.6 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 11 on page 33) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data for the CS42448 and operates in master or slave mode, generating either a 128Fs or 256Fs master clock on the RMCK output pin, and can operate in either the Left-Justified or I²S interface format.

Selections are made in the control port of the FPGA, accessible through the “FPGA” tab of the Cirrus Logic FlexGUI software. Refer to register “CS8416 Control (address 05h)” on page 21 for configuration settings.

1.7 CS5341

A complete description of the CS5341 Audio ADC (Figure 16 on page 38) is included in the CS5341 data sheet.

The CS5341 is connected to the AUX port of the CS42448 and is used only in the TDM interface format of the CODEC. The AUX port of the CS42448 masters the CS5341 and accepts either Left-Justified or I²S data on AUX_SDIN.

Selections are made in the control port of the FPGA, accessible through the “FPGA” tab of the Cirrus Logic FlexGUI software. Refer to register “CS5341 and Miscellaneous Control (Address 08h)” on page 26 for configuration settings.

1.8 Canned Oscillator

Oscillator Y1 provides a system master clock. This clock is routed through the CS8416 and out the RMCK pin when the S/PDIF input is disconnected (refer to the CS8416 data sheet for details on OMCK operation). To use the canned oscillator as the source of the MCLK signal, remove the S/PDIF input to the CS8416 and configure the CS8416 appropriately.

The oscillator is mounted in pin sockets, allowing easy removal or replacement.The board is shipped with a 12.2880 MHz crystal oscillator populated at Y1.

1.9 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J11 and J25.

The 24-pin, 2 row header, J25, provides access to the serial audio signals required to interface with a DSP (see Figure 13 on page 35).

Selections are made in the control port of the FPGA, accessible through the “FPGA” tab of the Cirrus Logic FlexGUI software. Refer to register “DSP Header Control (address 07h)” on page 24 for configuration settings

The 12-pin, 3 row header, J11, allows the user bidirectional access to the SPI/I^2C control signals by simply removing all the shunt jumpers from the “PC” position. The user may then choose to connect a ribbon cable to the “EXTERNAL” position. A single “GND” row for the ribbon cable’s ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I^2C power rail.

1.10 Analog Input

RCA connectors supply the CS42448 analog inputs through unity gain, AC-coupled single-ended to differential circuits. The inputs may also be driven single-ended by shunting the appropriate stake headers labeled “Single In”. A 1 Vrms single-ended signal into the RCA connectors will drive the CS42448 inputs to full scale.

1.11 Analog Outputs

The CS42448 analog outputs may be routed either through a single-pole RC passive filter, or a differential to single-ended 2-pole active filter.

1.12 Serial Control Port

A graphical user interface is included with the CDB42448 to allow easy manipulation of the registers in the CS42448 (see the CS42448 data sheet for register descriptions) and FPGA (see section 5 on page 16 for register descriptions). Connecting a cable to the RS-232 connector (J7) and launching the Cirrus Logic FlexGUI software will enable the CDB42448.

Refer to “Software Mode” on page 7 for a description of the Graphical User Interface (GUI).

1.13 USB Control Port

The USB control port connector (J12) is currently unavailable.

2. SOFTWARE MODE

The CDB42448 is shipped with a Microsoft Windows® based GUI, which allows control over the CS42448 and FPGA registers. Interface to the GUI is provided using an RS-232 serial cable. Once the appropriate cable is connected between the CDB42448 and the host PC, load "Flex-Loader.exe" from the CDB42448 directory. Once loaded, all registers are set to their default reset state. The GUI's "File" menu provides the ability to save and load script files containing all of the register settings. Sample script files are provided for basic functionality. Refer to section 3.1 on page 9 for details.

2.1 Advanced Register Debug Tab

The Advanced Register Debug tab provides low level control over the CS42448 and FPGA individual register settings. Each device is displayed on a separate tab. Register values can be modified bit-wise or byte-wise. For bit-wise, click the appropriate push button for the desired bit. For byte-wise, the desired hex value can be typed directly in the register address box in the register map.

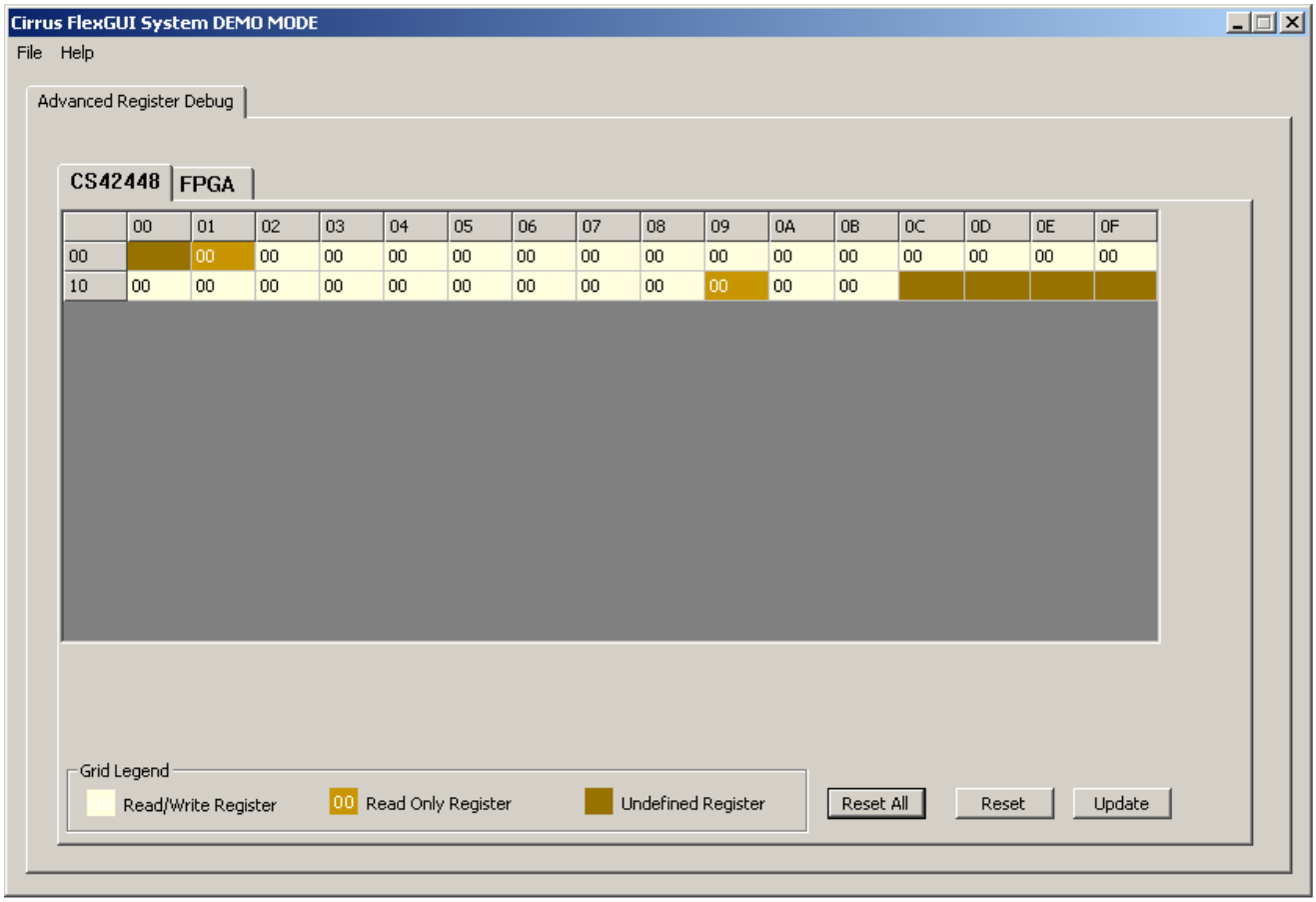

Figure 1. Advanced Register Tab - CS42448

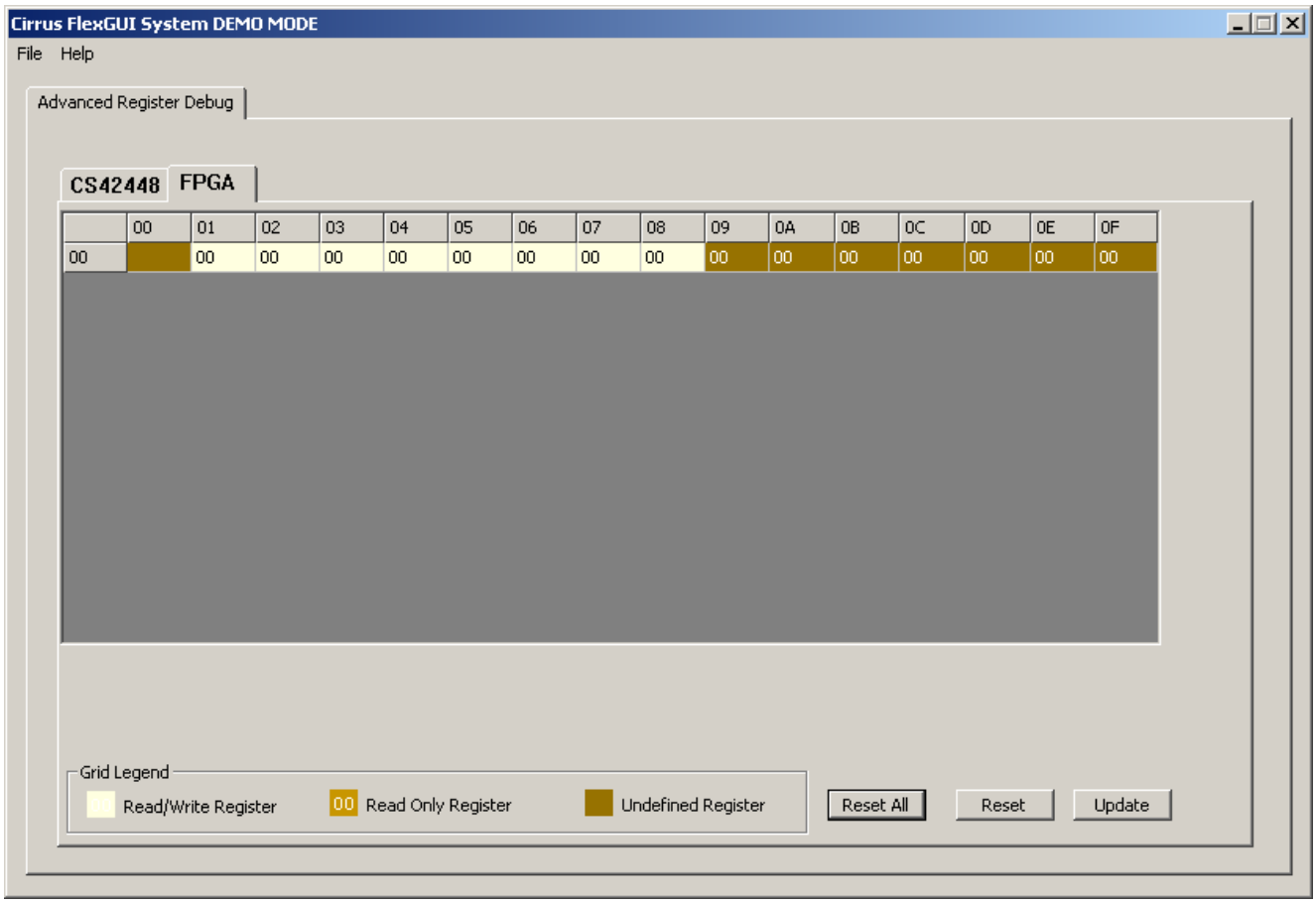

Figure 2. Advanced Register Tab - FPGA

3. FPGA SYSTEM OVERVIEW

The FPGA (U14) controls all digital signal routing between the CS42448, CS8406 CS8416, CS5341 and the DSP I/O Header. For easy evaluation of the TDM interface format of the CS42448, the FPGA will copy stereo PCM data from either the CS8416 or DSP I/O Header onto one data line at a 256Fs data rate. It will in turn de-multiplex the TDM data from the CS42448 and output stereo channel pairs to the CS8406.

3.1 FPGA Setup

Sections 3.2 to 3.4 show graphical descriptions of the routing topology internal to the FPGA. Section 3.5 shows the graphical description of the FPGA's control of the MCLK bus. And section 3.6 provides details for routing clocks and data, bypassing the FPGA (recommended for more advanced users only). Refer to "FPGA Register Description" on page 16 for all configuration settings.

The board may also be configured simply by choosing from 6 pre-defined scripts provided in the supplied CD ROM. The pre-defined scripts, along with a brief description, are shown below.

3.1.1 S/PDIF In, S/PDIF Out (SPDIF1-4)

This script sets up the CDB42448 to operate the CS8416 as the master and all other devices as slave. The CS8416 masters the MCLK bus.

Various permutations of this option exist as S/PDIF1, S/PDIF2, S/PDIF3 and S/PDIF4. Each permutation signifies which ADC data is transmitted to the CS8406.

The CS42448 operates in the TDM digital interface format. The FPGA copies PCM data from the CS8416 onto one data line and transmits this data to the DAC_SDIN1 input.

3.1.2 Analog In, Analog Out (Digital Loopback)

This script sets up the CDB42448 to operate the crystal oscillator as the master. The CS8416 passes the signal from the crystal oscillator, Y1, through its OMCK input and out its RMCK output (NOTE: the S/PDIF input must be disconnected). The CS8416 then generates sub clocks derived from the crystal oscillator and input to the FPGA for TDM clock generation. The FPGA then masters the sub clocks to the CS42448.

The CS42448 operates in the TDM digital interface format, looping ADC_SDOUT1 back into the DAC_SDIN1 input. ADC1-3 appear on DAC1-3 and the CS5341 ADC appears on DAC4.

3.1.3 DSP Routing

This script sets up the CDB42448 to operate the device attached to the DSP Header as the master and all other devices as slave. The DSP Header masters the MCLK bus.

3.2. Internal Sub-Clock Routing

The graphical description below shows the internal clock routing topology between the CS42448, CS8416, CS8406 and DSP Header. Refer to registers “CODEC Clock Control (address 03h)” on page 18, “CS8406 Control (address 04h)” on page 19 and “CS8416 Control (address 05h)” on page 21 for configuration settings.

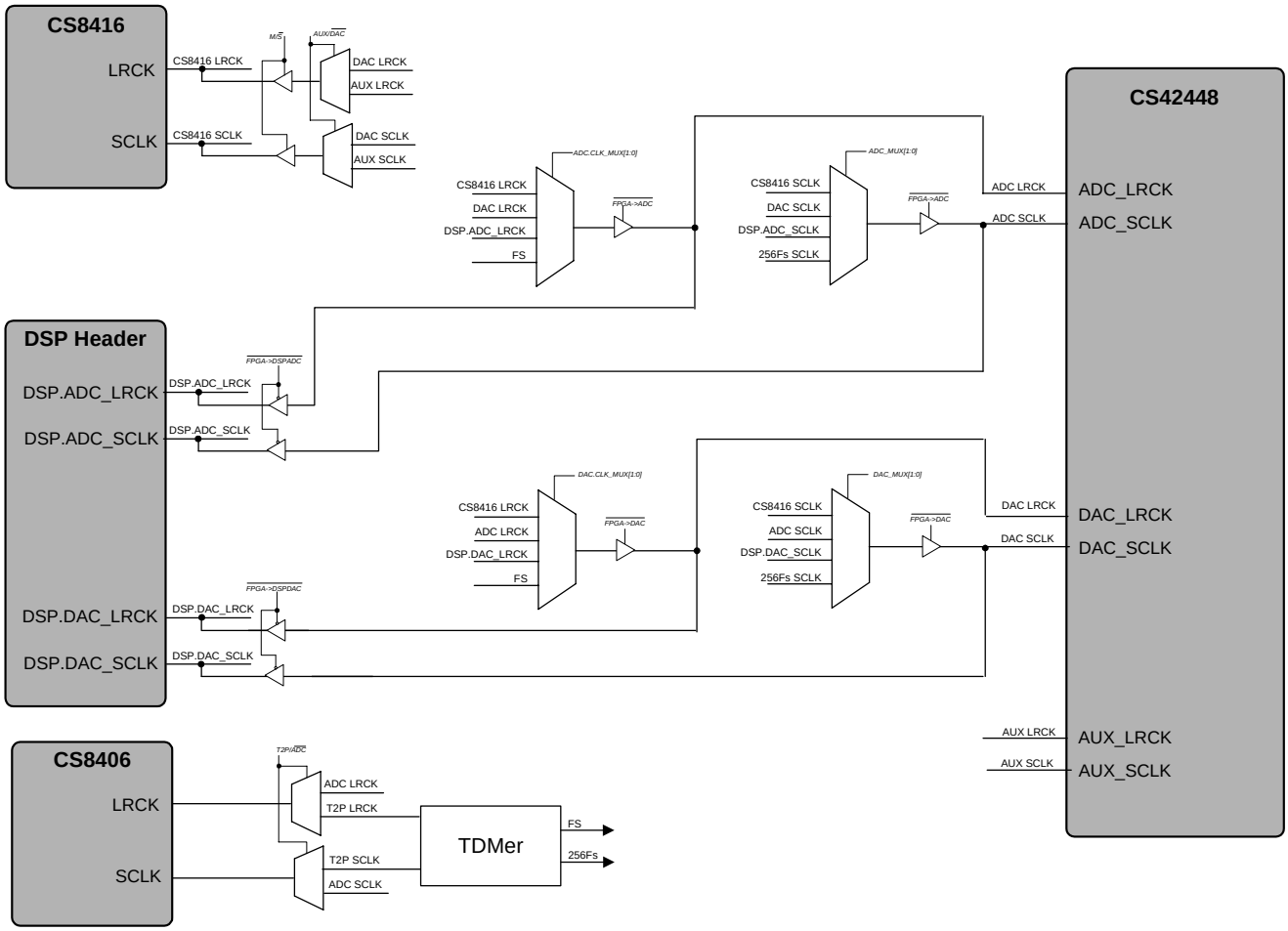

Figure 3. Internal Sub-Clock Routing

3.3. Internal Data Routing

The graphical description below shows the internal data routing topology between the CS42448, CS8416, CS8406 and DSP Header. Refer to registers “CODEC SDINx Control (address 02h)” on page 17, “CS8406 Control (address 04h)” on page 19 and “DSP Header Control (address 07h)” on page 24 for configuration settings.

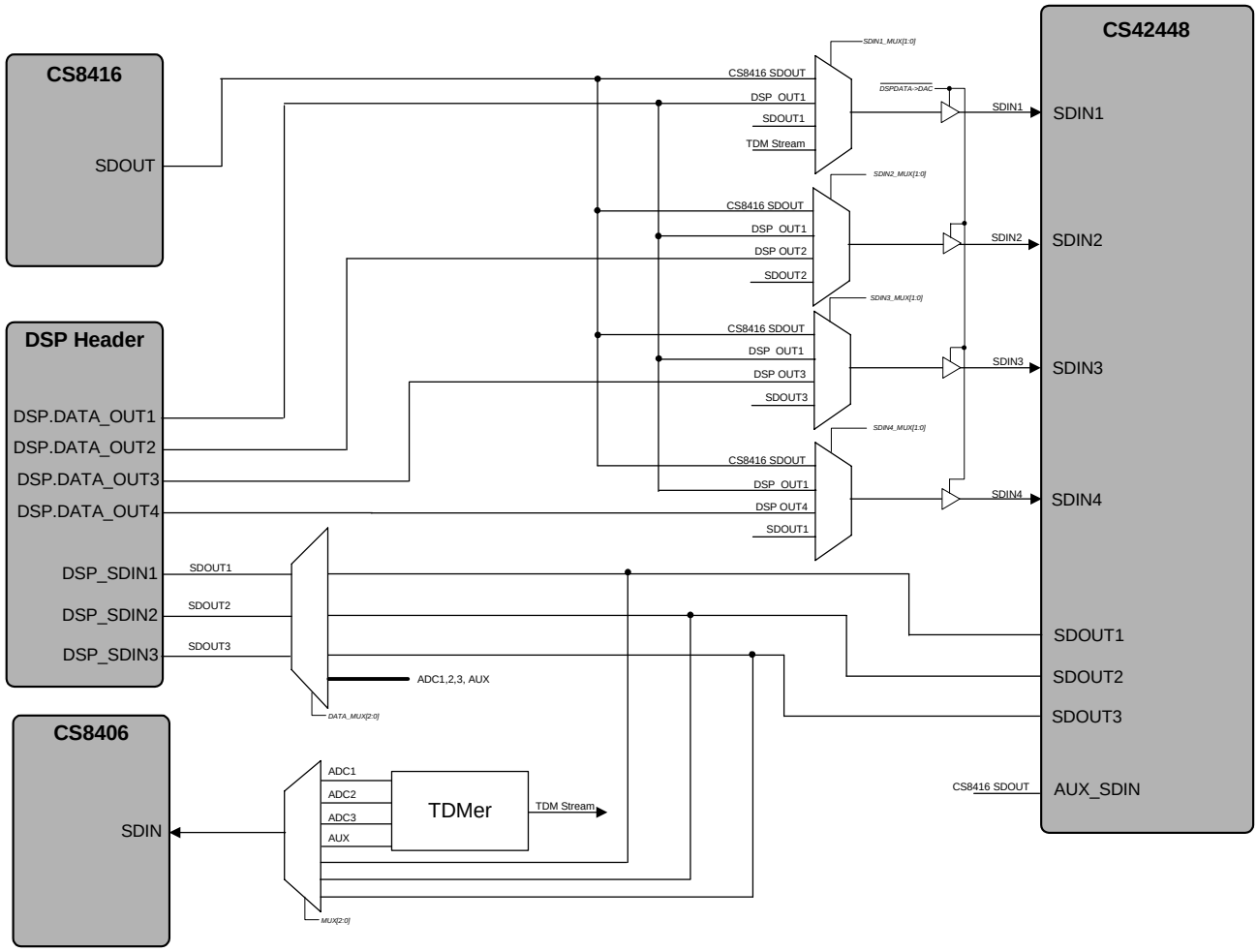

Figure 4. Internal Data Routing

3.4. Internal TDM Conversion, MUXing and Control (TDMer)

The graphical description below shows the routing topology of the TDM converter between the CS42448, CS8416, CS8406 and DSP Header. Refer to register “TDM Conversion (address 01h)” on page 16 for configuration settings.

The TDMer allows the user to easily evaluate the CS42448 in the TDM digital interface format. A 256Fs clock and an FS pulse is derived from either the CS8416 or DSP Header. Data is multiplexed onto one data line and transmitted to the DAC. Likewise, data from the ADC of the CS42448 is de-multiplexed and transmitted to the CS8406. The CS8406 sub clocks, in this case, must be taken from the TDM2PCM engine of the TDMer (refer to register “ADC or TDM2PCM Clock Selection (T2P/ADC)” on page 20 for implementation).

The TDMer is also capable of transmitting the de-multiplexed data to the DSP Header; however, the user must re-time this data using a DSP. The CDB42448 does not provide an option for routing the TDM2PCM clocks to the DSP Header.

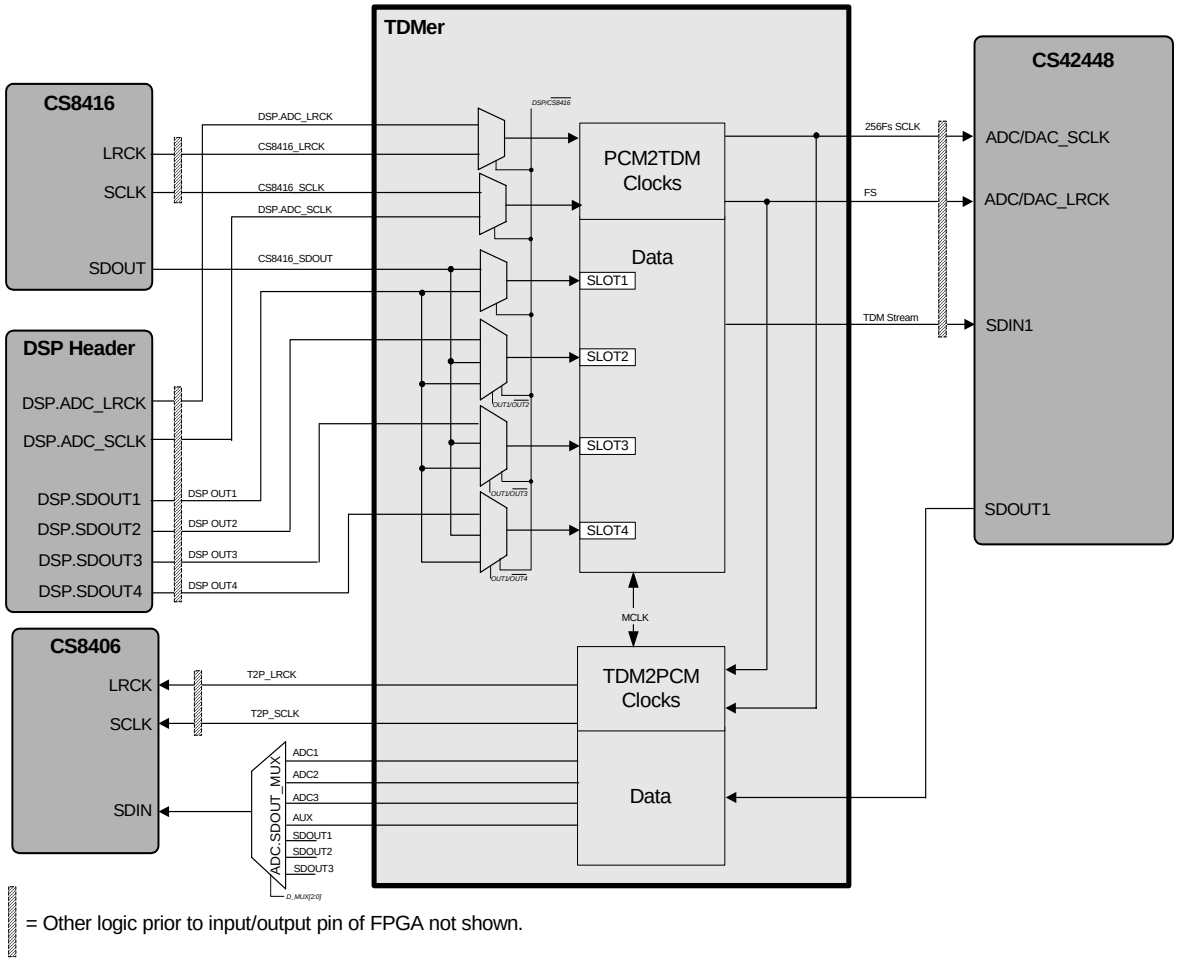

Figure 5. TDMer

3.5 External MCLK Control

Several sources for MCLK exist on the CDB42448. The crystal oscillator, Y1, will master the MCLK bus when no S/PDIF signal is input to the CS8416 (refer to the CS8416 data sheet for details on OMCK operation). This signal will be driven directly out the CS8416.

The CS8416 will generate a master clock whenever its internal PLL is locked to the incoming S/PDIF stream. This MCLK signal from the CS8416 can be taken off the MCLK bus by setting the "RMCK_Master" bit in the register "CS8416 Control (address 05h)" on page 21.

The DSP Header can master or slave the MCLK bus by setting the "MCLK_M/$\overline{S}$" bit in the register "DSP Header Control (address 07h)" on page 24 accordingly.

3.5.1 CS5341 MCLK

To accommodate an MCLK signal greater than 25 MHz on the MCLK bus, a 2.0 divider internal to the FPGA has been implemented. The divided MCLK signal is routed only to the CS5341. Refer to register "CS5341 and Miscellaneous Control (Address 08h)" on page 26 for the required setting.

3.5.2 TDMer MCLK

MCLK signals greater than 256Fs must be divided accordingly to maintain a 256Fs MCLK signal into the TDMer. A 1.5 and a 2.0 divider has been implemented inside the FPGA. Refer to register "CS5341 and Miscellaneous Control (Address 08h)" on page 26 for the required setting.

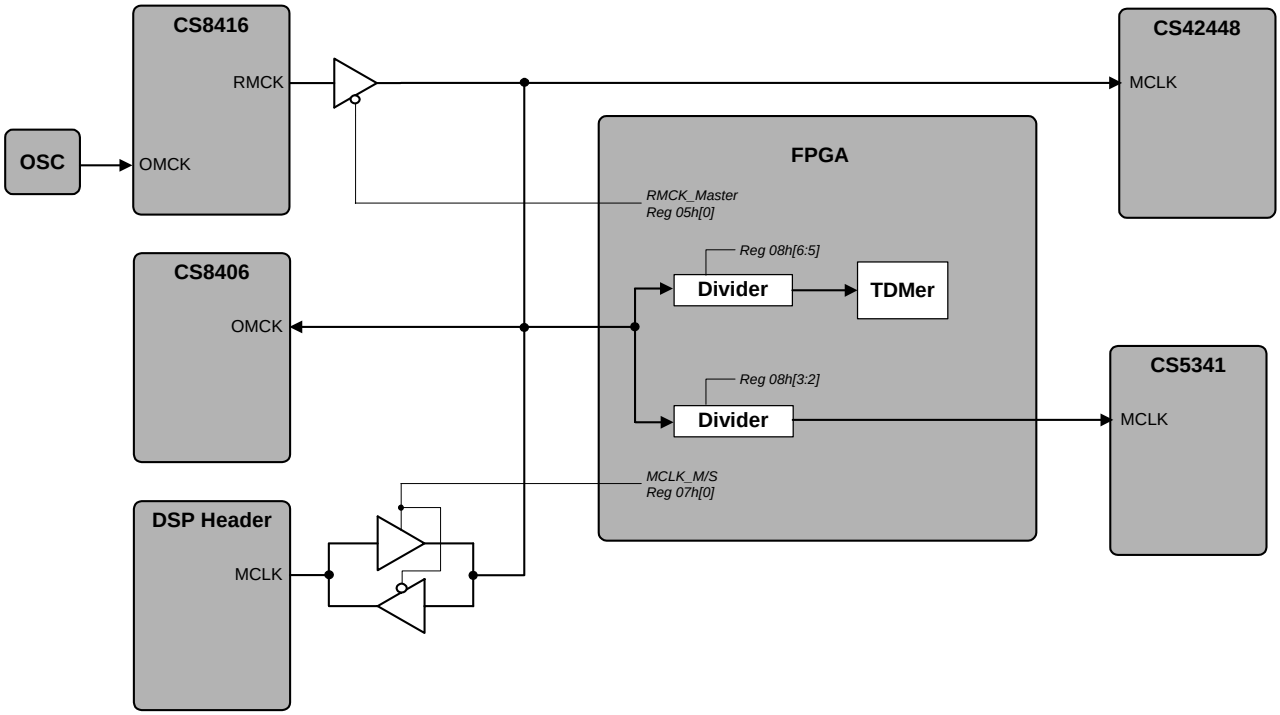

Figure 6. External MCLK Control

3.6 Bypass Control - Advanced

The DSP clocks and data may be routed through buffers directly to the CS42448, bypassing the FPGA. This configuration may be desired for more stringent timing requirements at higher clock speeds. See register “Bypass Control (address 06h)” on page 22. These bits are only accessible through the Advanced tab of the Cirrus Logic FlexGui software.

NOTE: To avoid contention with the FPGA, set the clock direction for the FPGA appropriately: The $\overline{\text{FPGA->DAC}}$ and $\overline{\text{FPGA->ADC}}$ bits in register 03h and 07h must be set to ‘1’b.

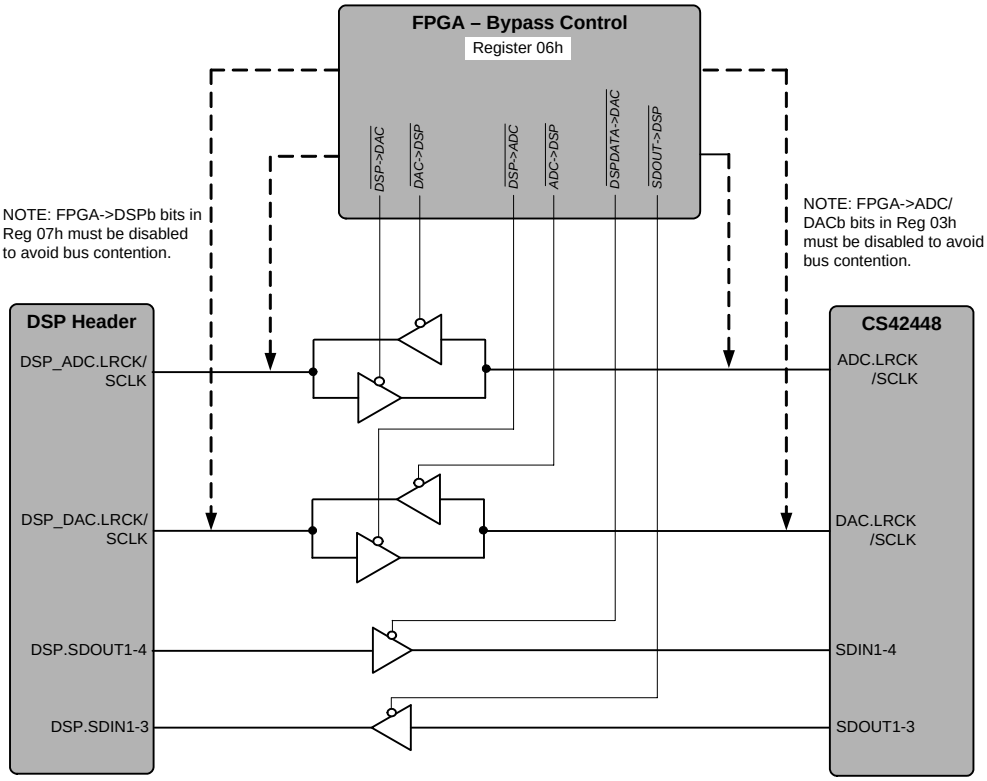

Figure 7. Bypass FPGA Control

4. FPGA REGISTER QUICK REFERENCE

	Function	7	6	5	4	3	2	1	0
01h	TDM Conversion	DSP/$\overline{\text{CS8416}}$	OUT1/$\overline{\text{OUT2}}$	OUT1/$\overline{\text{OUT3}}$	OUT1/$\overline{\text{OUT4}}$	Reserved	Reserved	Reserved	PDN_TDMer
	p 16 default	0	0	0	0	0	0	0	0
02h	CODEC SDINx Control	SDIN4.MUX1	SDIN4.MUX0	SDIN3.MUX1	SDIN3.MUX0	SDIN2.MUX1	SDIN2.MUX0	SDIN1.MUX1	SDIN1.MUX0
	p 17 default	1	1	1	1	1	1	1	0
03h	CODEC Clock Control	Reserved	Reserved	DAC.CLK_MUX1	DAC.CLK_MUX0	$\overline{\text{FPGA->DAC}}$	ADC.CLK_MUX1	ADC.CLK_MUX0	$\overline{\text{FPGA->ADC}}$
	p 18 default	0	0	1	1	0	1	1	0
04h	CS8406 Control	Reserved	$\overline{\text{RST}}$	MUX2	MUX1	MUX0	128/$\overline{\text{256}}$ Fs	I²S/$\overline{\text{LJ}}$	T2P/$\overline{\text{ADC}}$
	p 19 default	0	1	1	0	0	0	0	1
05h	CS8416 Control	Reserved	Reserved	AUX/$\overline{\text{DAC}}$	$\overline{\text{RST}}$	M/$\overline{\text{S}}$	128/$\overline{\text{256}}$ Fs	I²S/$\overline{\text{LJ}}$	RMCK_$\overline{\text{Master}}$
	p 21 default	0	0	1	1	1	0	0	0
06h	Bypass Control	Reserved	$\overline{\text{DSPDATA->DAC}}$	$\overline{\text{SDOUT->DSP}}$	$\overline{\text{CS5341->AUX}}$	$\overline{\text{DAC->DSP}}$	$\overline{\text{ADC->DSP}}$	$\overline{\text{DSP->DAC}}$	$\overline{\text{DSP->ADC}}$
	p 22 default	1	1	1	0	1	1	1	1
07h	DSP Header Control	Reserved	Reserved	DATA_MUX2	DATA_MUX1	DATA_MUX0	$\overline{\text{FPGA->DAC}}$	$\overline{\text{FPGA->ADC}}$	MCLK_M/$\overline{\text{S}}$
	p 24 default	0	0	0	0	0	0	1	0
08h	CS5341/Misc Control	Reserved	Reserved	INT.MCLK_DIV	OMCK/DIV_1.5/2	‘41_MCLK_DIV	‘41_DIV_1.5/2	‘41_I²S/$\overline{\text{LJ}}$	‘41_$\overline{\text{RST}}$
	p 26 default	0	1	0	0	0	0	0	1

5. FPGA REGISTER DESCRIPTION

All registers are read/write. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

5.1 TDM CONVERSION (ADDRESS 01H)

7	6	5	4	3	2	1	0
DSP/$\overline{\text{CS8416}}$	OUT1/$\overline{\text{OUT2}}$	OUT1/$\overline{\text{OUT3}}$	OUT1/$\overline{\text{OUT4}}$	Reserved	Reserved	Reserved	PDN_TDMer

5.1.1 PCM2TDM CLOCK SELECTION (DSP/$\overline{\text{CS8416}}$)

Default = 0
0 - CS8416
1- DSP_ADC Header

Function:

This bit selects the clock source for the PCM2TDM (P2T) converter. It also selects the data source for Slot 1 (see Figure 5 on page 12) of the TDMer.

This bit also serves as the MSB of the 3:2 data selection MUX's for slots 2-4 of the TDM Stream (see Figure 5 on page 12).

5.1.2 PCM2TDM DATA SELECTION (OUT1/$\overline{\text{OUTX}}$)

Default = 0
0 - OUTx
1- OUT1

Function:

This bit selects the data source for the PCM2TDM (P2T) converter. The DSP/$\overline{\text{CS8416}}$ bit serves as the MSB of the MUX that selects between OUTx and OUT1.

If the CS8416 is selected as the clock source for the P2T converter, this bit is ignored and the CS8416 SDOUT will be selected as the data source for slots 2-4 (see Figure 5 on page 12).

5.1.3 POWER DOWN TDM CONVERTER (PDN_TDMER)

Default = 0
0 - Disabled
1- Enabled

Function:

This bit powers down the TDMer.

5.2 CODEC SDINX CONTROL (ADDRESS 02H)

7	6	5	4	3	2	1	0
SDIN4.MUX1	SDIN4.MUX0	SDIN3.MUX1	SDIN3.MUX0	SDIN2.MUX1	SDIN2.MUX0	SDIN1.MUX1	SDIN1.MUX0

5.2.1 SDIN4 MUX(SDIN4.MUX)

Default = 11

SDIN4.MUX[1:0]	Data Selection
00	CS8416 SDOUT
01	DSP SDOUT1
10	DSP SDOUT4
11	ADC_SDOUT1

Table 1. Data to SDIN4

Function:

This MUX selects the data lines from the CS8416, DSP Header, and the ADC (see Figure 4 on page 11).

5.2.2 SDIN3 MUX(SDIN3.MUX)

Default = 11

SDIN3.MUX[1:0]	Data Selection
00	CS8416 SDOUT
01	DSP SDOUT1
10	DSP SDOUT3
11	ADC_SDOUT3

Table 2. Data to SDIN3

Function:

This MUX selects the data lines from the CS8416, DSP Header, and the ADC (see Figure 4 on page 11).

5.2.3 SDIN2 MUX(SDIN2.MUX)

Default = 11

SDIN2.MUX[1:0]	Data Selection
00	CS8416 SDOUT
01	DSP SDOUT1
10	DSP SDOUT2
11	ADC_SDOUT2

Table 3. Data to SDIN2

Function:

This MUX selects the data lines from the CS8416, DSP Header, and the ADC (see Figure 4 on page 11).

5.2.4 SDIN1 MUX(SDINX.MUX)

Default = 10

SDIN1.MUX[1:0]	Data Selection
00	CS8416 SDOUT
01	DSP_ SDOUT1
10	ADC_SDOUT1
11	TDM Stream

Table 4. Data to SDIN1

Function:

This MUX selects the data lines from the CS8416, DSP Header, the ADC and the TDM Stream from the TDMer (see Figure 4 on page 11).

5.3 CODEC CLOCK CONTROL (ADDRESS 03H)

7	6	5	4	3	2	1	0
Reserved	Reserved	DAC.CLK_ MUX1	DAC.CLK_ MUX0	$\overline{\text{FPGA->DAC}}$	ADC.CLK_ MUX1	ADC,CLK_ MUX0	$\overline{\text{FPGA->ADC-CODEC}}$

5.3.1 DAC CLOCK MUX (DAC.CLK_MUX[1:0])

Default = 11

DAC.CLK_ MUX[1:0]	Clock Selection
00	CS8416
01	ADC
10	DSP DAC
11	TDMer

Table 5. Clocks to DAC

Function:

This MUX selects the sub-clock lines from the CS8416, ADC, DSP Header and the sub-clocks from the TDMer internal to the FPGA (see Figure 3 on page 10).

5.3.2 FPGA CLOCKS TO DAC CLOCKS ($\overline{\text{FPGA->DAC}}$)

Default = 0
0 - FPGA Masters DAC clock bus
1 - FPGA Slave to DAC clock bus

Function:

This bit toggles a control line for the internal clock buffer to the DAC serial port (see Figure 3 on page 10) .

5.3.3 ADC MUX (ADC.CLK_MUX)

Default = 11

ADC.CLK_ MUX[1:0]	Clock Selection
00	CS8416
01	DAC
10	DSP ADC
11	TDMer

Table 6. Clocks to ADC

Function:

This MUX selects the sub-clock lines from the CS8416, DAC, DSP Header and the sub-clocks from the TDMer internal to the FPGA (see Figure 3 on page 10).

5.3.4 FPGA CLOCKS TO ADC CLOCKS ($\overline{\text{FPGA->ADC}}$)

Default = 0
0 - FPGA Masters ADC clock bus
1 - FPGA Slave to ADC clock bus

Function:

This bit toggles a control line for the internal clock buffer to the ADC serial port (see Figure 3 on page 10).

5.4 CS8406 CONTROL (ADDRESS 04H)

7	6	5	4	3	2	1	0
Reserved	$\overline{\text{RST}}$	MUX2	MUX1	MUX0	128/$\overline{256}$ Fs	I²S/$\overline{\text{LJ}}$	T2P/$\overline{\text{ADC}}$

5.4.1 RESET ($\overline{\text{RST}}$)

Default = 1
0 - CS8406 held in reset
1 - CS8406 taken out of reset

Function:

This bit is used to reset the CS8406 and is held low for 300 μs upon FPGA initialization.

5.4.2 DATA MUX(MUX)

Default = 100

MUX[2:0]	Data Selection
000	ADC_SDOUT
001	ADC_SDOUT2
010	ADC_SDOUT3
011	ADC_SDOUT1

Table 7. Data to CS8406

MUX[2:0]	Data Selection
100	ADC1 (from ADC_SDOUT1)
101	ADC2 (from ADC_SDOUT1)
110	ADC3 (from ADC_SDOUT1)
111	EXT_ADC (from ADC_SDOUT1)

Table 7. Data to CS8406

Function:

This MUX selects the data lines from the ADC's and the external ADC. The first 4 selections shown in Table 7 comes directly from the data output lines. The last 4 selections are de-multiplexed from the TDM stream of SDOUT1 (see Figure 5 on page 12).

5.4.3 OMCK/LRCK RATIO SELECT (OMCK 128/$\overline{256}$ FS)

Default = 0
0 - 256 Fs
1 - 128 Fs

Function:

Selects the MCLK/LRCK ratio of the CS8406 transmitter.

5.4.4 LEFT-JUSTIFIED OR I^{2}S INTERFACE FORMAT (I^{2}S/$\overline{LJ}$)

Default = 0
0 - Left Justified
1 - I^{2}S

Function:

Selects either I^{2}S or Left Justified interface format for the CS8406.

5.4.5 ADC OR TDM2PCM CLOCK SELECTION (T2P/$\overline{ADC}$)

Default = 1
0 - ADC Sub-Clocks to CS8406
1 - TDMer Sub-Clocks to CS8406

Function:

Selects the clock source for the CS8406. When de-multiplexing the data on SDOUT1, the CS8406 will need to use the TDMer sub-clocks (see Figure 3 on page 10).

5.5 CS8416 CONTROL (ADDRESS 05H)

7	6	5	4	3	2	1	0
Reserved	Reserved	AUX/$\overline{\text{DAC}}$	$\overline{\text{RST}}$	M/$\overline{\text{S}}$	128/$\overline{\text{256}}$ Fs	I²S/$\overline{\text{LJ}}$	$\overline{\text{RMCK\_Master}}$

5.5.1 AUX OR DAC CLOCK SELECTION (AUX/$\overline{\text{DAC}}$)

Default = 1
0 - DAC Sub-Clocks to CS8416
1 - AUX Sub-Clocks to CS8416

Function:

Selects the clock source for the CS8416 when in slave mode (see Figure 3 on page 10).

5.5.2 RESET ($\overline{\text{RST}}$)

Default = 1
0 - CS8416 held in reset
1 - CS8416 taken out of reset

Function:

This bit is used to reset the CS8416 and is held low for 300 μs upon FPGA initialization. It is also pulled low for 300 μs whenever registers 05h[3:1] change.

5.5.3 MASTER/SLAVE SELECT (M/$\overline{\text{S}}$)

Default = 1
0 - Slave
1 - Master

Function:

Selects master/slave mode for the CS8416 and configures the internal routing buffers. Pin 6 ($\overline{\text{RST}}$ bit) is held low for 300 μs whenever this bit changes.

5.5.4 RMCK/LRCK RATIO SELECT (128/$\overline{\text{256}}$ FS)

Default = 0
0 - 256 Fs
1 - 128 Fs

Function:

Selects the RMCK/LRCK ratio for the CS8416. Pin 6 ($\overline{\text{RST}}$ bit) is held low for 300 μs whenever this bit changes.

5.5.5 LEFT-JUSTIFIED OR I²S INTERFACE FORMAT (I²S/$\overline{LJ}$)

Default = 0
0 - Left-Justified
1 - I²S

Function:

Selects either I²S or Left Justified interface format for the CS8416. Pin 6 ($\overline{RST}$ bit) is held low for 300 µs whenever this bit changes.

5.5.6 RMCK MASTERS MCLK BUS ($\overline{RMCK\_MASTER}$)

Default = 0
0 - Enabled
1 - Disabled

Function:

Enables/disables the external MCLK output buffer on the MCLK bus (see Figure 6 on page 13).

5.6 BYPASS CONTROL (ADDRESS 06H)

7	6	5	4	3	2	1	0
Reserved	$\overline{DSPDATA}$ ->$\overline{DAC}$	$\overline{SDOUT->DSP}$	$\overline{CS5341}$ ->$\overline{AUX}$	$\overline{DAC->DSP}$	$\overline{ADC->DSP}$	$\overline{DSP->DAC}$	$\overline{DSP->ADC}$

NOTE: To avoid contention with the FPGA, set the clock direction for the FPGA appropriately: $\overline{FPGA->DAC}$ and $\overline{FPGA->ADC}$ in register 03h and 07h must be set to '1'b.

5.6.1 DSP DATA ROUTE TO DAC ($\overline{DSPDATA->DAC}$)

Default = 1
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the data buffer external to the FPGA to route the DSP Data directly to the DAC (see Figure 7 on page 14). The inverted signal controls active low buffers internal to the FPGA that routes the FPGA data to the DAC. Refer to Figure 4 on page 11.

5.6.2 ADC SDOUT DATA ROUTE TO DSP ($\overline{SDOUT->DSP}$)

Default = 1
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the external data buffer to route the ADC Data directly to the DSP (see Figure 7 on page 14). The inverted signal controls active low buffers external to the FPGA that

routes the FPGA data to the DSP. Refer to schematic Figure 14 on page 36.

5.6.3 ADC TO AUX SDIN ($\overline{\text{CS5341->AUX}}$)

Default = 0
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the external data buffer to route the external ADC Data directly to the AUX_SDIN port. When disabled, the FPGA will route the CS8416 SDOUT to the AUX_SDIN port.

5.6.4 DAC CLOCKS TO DSP ($\overline{\text{DAC->DSP}}$)

Default = 1
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the external clock buffer to route the DAC sub clocks directly to the DSP port (see Figure 7 on page 14).

5.6.5 ADC CLOCKS TO DSP ($\overline{\text{ADC->DSP}}$)

Default = 1
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the external clock buffer to route the ADC sub clocks directly to the DSP port (see Figure 7 on page 14).

5.6.6 DSP CLOCKS TO DAC ($\overline{\text{DSP->DAC}}$)

Default = 1
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the external clock buffer to route the DSP clocks directly to the DAC serial port (see Figure 7 on page 14).

5.6.7 DSP CLOCKS TO ADC ($\overline{\text{DSP->ADC}}$)

Default = 1
0 - Enable
1 - Disable

Function:

This bit toggles a control line for the external clock buffer to route the DSP clocks directly to the ADC serial port (see Figure 7 on page 14).

5.7 DSP HEADER CONTROL (ADDRESS 07H)

7	6	5	4	3	2	1	0
Reserved	Reserved	DATA_MUX2	DATA_MUX1	DATA_MUX0	$\overline{\text{FPGA->DSPDAC}}$	$\overline{\text{FPGA->DSPADC}}$	MCLK_M/$\overline{\text{S}}$

5.7.1 DATA MUX(DATA_MUX[2:0])

Default = 000

	DSP Data Selection		
MUX[2:0]	**DSP.SDIN1**	**DSP.SDIN2**	**DSP.SDIN3**
000	SDOUT1	SDOUT2	SDOUT3
001	ADC1 (from SDOUT1)	ADC2 (from SDOUT1)	ADC3 (from SDOUT1)
010	ADC2 (from SDOUT1)	ADC3 (from SDOUT1)	EXT_ADC (from SDOUT1)
011	ADC3 (from SDOUT1)	EXT_ADC (from SDOUT1)	ADC1 (from SDOUT1)
100	EXT_ADC (from SDOUT1)	ADC1 (from SDOUT1)	ADC2 (from SDOUT1)
101	ADC1 (from SDOUT1)	ADC1 (from SDOUT1)	ADC1 (from SDOUT1)
110	ADC2 (from SDOUT1)	ADC2 (from SDOUT1)	ADC2 (from SDOUT1)
111	ADC3 (from SDOUT1)	ADC3 (from SDOUT1)	ADC3 (from SDOUT1)

Table 8. Data to DSP

Function:

This MUX selects the data lines from the ADC's and the external ADC. The first selection shown in Table 8 comes directly from data output lines. The last 7 are de-multiplexed from the TDM data stream (NOTE: in this latter scenario, the data will need to be re-timed from the TDMer's sub clocks). Refer to Figure 4 on page 11.

5.7.2 FPGA TO DSP_DAC CLOCKS ($\overline{\text{FPGA->DSPDAC}}$)

Default = 0
0 - FPGA Masters DSP_DAC clock bus
1 - FPGA Slave to DSP_DAC clock bus

Function:

This bit toggles a control line for the internal and external clock buffers for the DSP DAC headers (see Figure 3 on page 10).

5.7.3 FPGA TO DSP_ADC CLOCKS ($\overline{\text{FPGA->DSPADC}}$)

Default = 1
0 - FPGA Masters DSP_ADC clock bus
1 - FPGA Slave to DSP_ADC clock bus

Function:

This bit toggles a control line for the external clock buffer for the DSP ADC headers (see Figure 3 on

page 10).

5.7.4 DSP MCLK (MCLK_M/$\overline{S}$)

Default = 0
0 - DSP MCLK is a slave to the MCLK bus.
1 - DSP MCLK masters MCLK bus.

Function:

Enables/disables the external DSP MCLK output buffer on the MCLK bus.

5.8 CS5341 AND MISCELLANEOUS CONTROL (ADDRESS 08H)

7	6	5	4	3	2	1	0
Reserved	Reserved	INT.MCLK_ DIV	INT.DIV_ 1.5/2	'41_MCLK_ DIV	'41_DIV_ 1.5/2	'41_I²S/$\overline{LJ}$	'41_$\overline{RST}$

5.8.1 INT MCLK DIVIDE (1.5/2.0 DIVIDE)

Default = 0
0 - Disabled
1 - Enabled

Function:

Enables/disables the internal (1.5 or 2.0) divide circuitry for MCLK.

5.8.2 1.5 OR 2.0 MCLK DIVIDE (1.5/2.0 DIVIDE)

Default = 0
0 - Divide by 1.5
1 - Divide by 2.0

Function:

Divides the internal MCLK by 1.5 or 2 to all internal logic. This is intended to accommodate an external MCLK that is greater than 256 Fs. SCLK is derived from MCLK and must always be 256Fs in TDM Mode (see Figure 6 on page 13).

5.8.3 EXT MCLK DIVIDE ('41_MCLK_DIV)

Default = 0
0 - Disabled
1 - Enabled

Function:

Enables/disables the internal (1.5 or 2.0) divide circuitry for the CS5341 MCLK.

5.8.4 1.5 OR 2.0 CS5341 MCLK DIVIDE ('41_DIV_1.5/2.0)

Default = 0
0 - Divide by 1.5
1 - Divide by 2.0

Function:

Divides the MCLK from the MCLK bus to the CS5341 by 1.5 or 2 (see Figure 6 on page 13).

5.8.5 LEFT-JUSTIFIED OR I^2S INTERFACE FORMAT ('41_$I^2S/\overline{LJ}$)

Default = 0
0 - Left Justified
1 - I^2S

Function:

Selects either I^2S or Left Justified interface format for the CS5341. Reset to the CS5341 is toggled.

5.8.6 RESET (‘41_$\overline{\text{RST}}$)

Default = 1
0 - CS5341 is held in reset
1 - CS5341 is taken out of reset

Function:

This bit toggles pin 30 of the FPGA and is held low for 300 μs upon FPGA initialization. It will also be held low for 300 μs whenever register 08h[1] changes.

6. CDB CONNECTORS AND JUMPERS

CONNECTOR	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J2	Input	+5.0 V Power Supply
+12V	J5	Input	+12.0 V Power Supply
-12V	J4	Input	-12.0 V Power Supply
GND	J3	Input	Ground Reference
SPDIF OPTICAL OUT	J14	Output	CS8406 digital audio output via optical cable
SPDIF COAX OUT	J18	Output	CS8406 digital audio output via coaxial cable
SPDIF OPTICAL IN	J21	Input	CS8416 digital audio input via optical cable
SPDIF COAX IN	J18	Input	CS8416 digital audio input via coaxial cable
RS232	J7	Input/Output	Serial connection to PC for SPI / I^2C control port signals
USB	J12	Input/Output	USB connection to PC for SPI / I^2C control port signals. **Not Available.**
DSP Header	J25	Input/Output	I/O for Clocks & Data
CONTROL	J11	Input/Output	I/O for external SPI / I^2C control port signals.
USB JTAG	J8	Input/Output	I/O for programming the micro controller (U8).
FPGA JTAG	J10	Input/Output	I/O for programming the FPGA (U14).
USB RESET	S1	Input	Reset for the micro controller (U8).
FPGA RESET	S2	Input	Reset for the FPGA (U14).
AIN1 AIN2 AIN3 AIN4 AIN5-/5B AIN5+/5A AIN6-/6B AIN6+/6A	J37 J27 J22 J17 J15 J13 J9 J6	Input	RCA phono jacks for analog input signal to CS42448.
AIN7 AIN8	J28 J38	Input	RCA phono jacks for analog input signal to CS5341.
AOUT1 AOUT2 AOUT3 AOUT4 AOUT5 AOUT6 AOUT7 AOUT8	J47 J48 J49 J50 J51 J52 J53 J54	Output	RCA phono jacks for analog outputs.

Table 9. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J1	Selects source of voltage for the VA supply	+3.3V *+5V	Voltage source is +3.3 V regulator Voltage source is +5 V regulator
AIN1- (J26)	Selects the negative leg of the single-ended to differential input circuit in differential mode, or a VA/2 bias in single-ended mode.	*DIFF IN SINGLE IN	Inverted signal from AIN1 input VA/2 voltage bias
AIN2- (J23)	Selects the negative leg of the single-ended to differential input circuit in differential mode, or a VA/2 bias in single-ended mode.	*DIFF IN SINGLE IN	Inverted signal from AIN2 input VA/2 voltage bias
AIN3- (J19)	Selects the negative leg of the single-ended to differential input circuit in differential mode, or a VA/2 bias in single-ended mode.	*DIFF IN SINGLE IN	Inverted signal from AIN3 input VA/2 voltage bias
AIN4- (J16)	Selects the negative leg of the single-ended to differential input circuit in differential mode, or a VA/2 bias in single-ended mode.	*DIFF IN SINGLE IN	Inverted signal from AIN4 input VA/2 voltage bias
J29-J36 J39-J46	Selects between an active or a passive analog output filter for AOUT1-8.	*A P	2-Pole Active Filter Single-Pole Passive Filter

*Default factory settings

Table 10. Jumper Settings

7. CDB BLOCK DIAGRAM

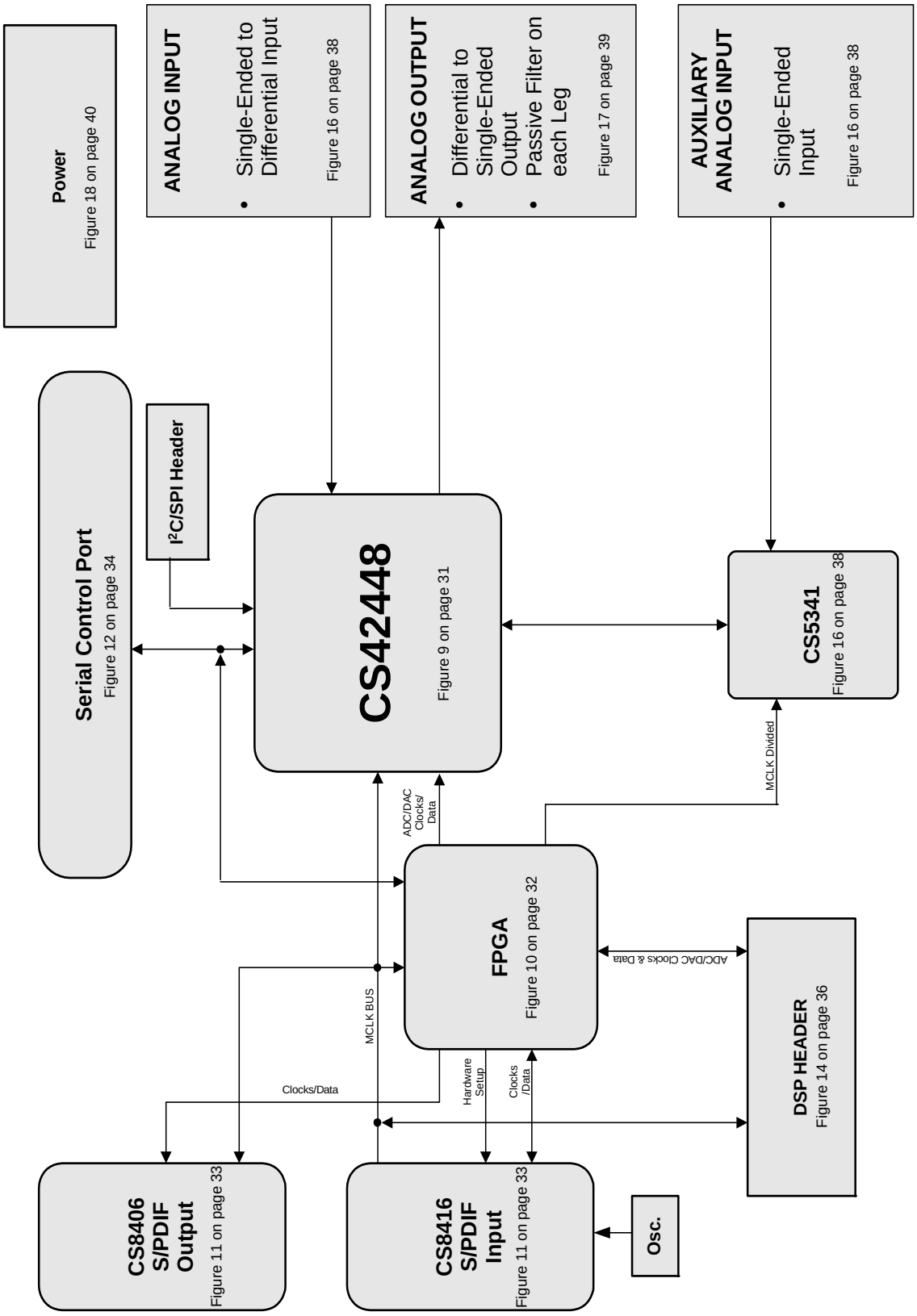

Figure 8. Block Diagram

8. CDB SCHEMATICS

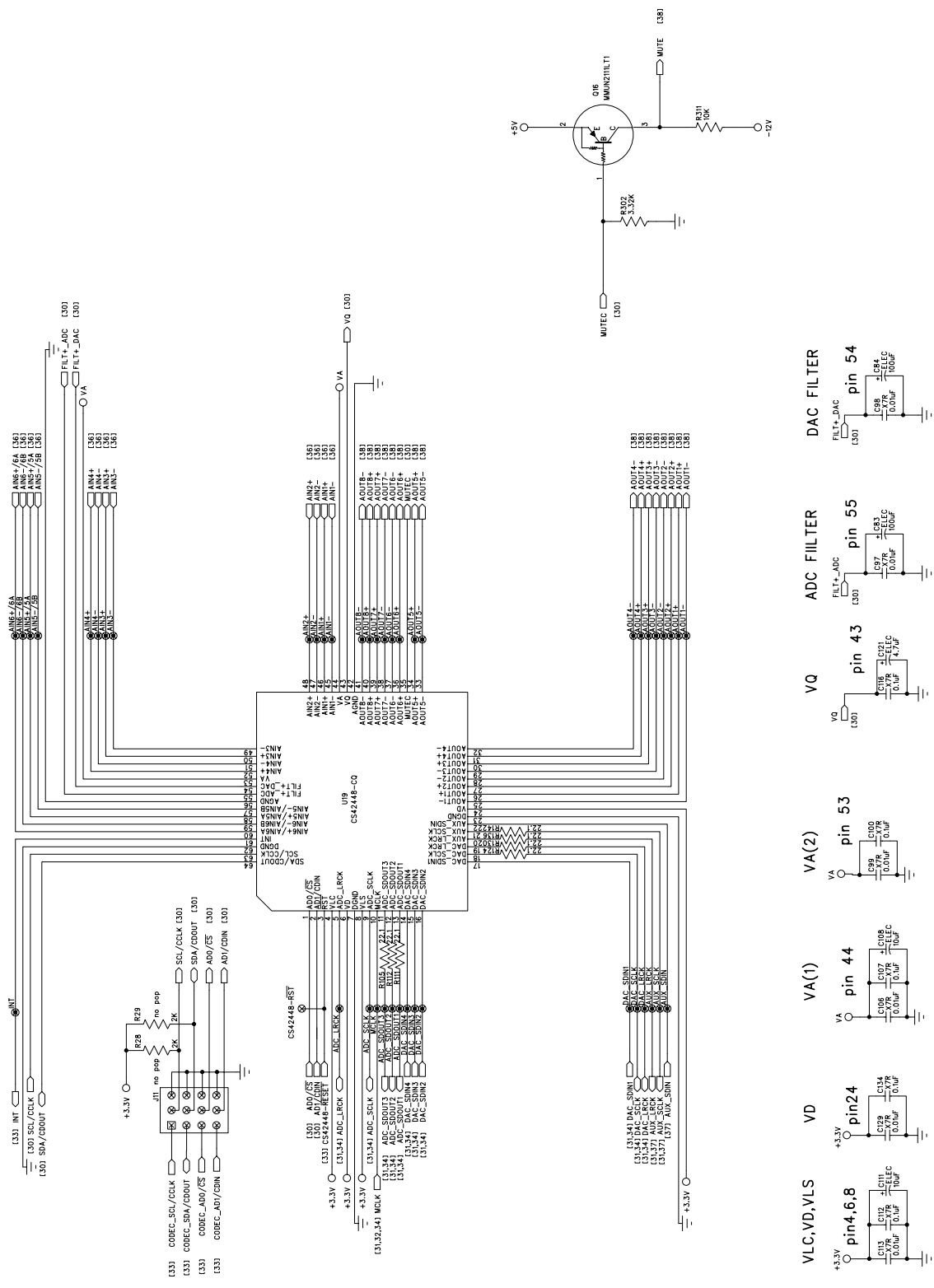

Figure 9. CS42448

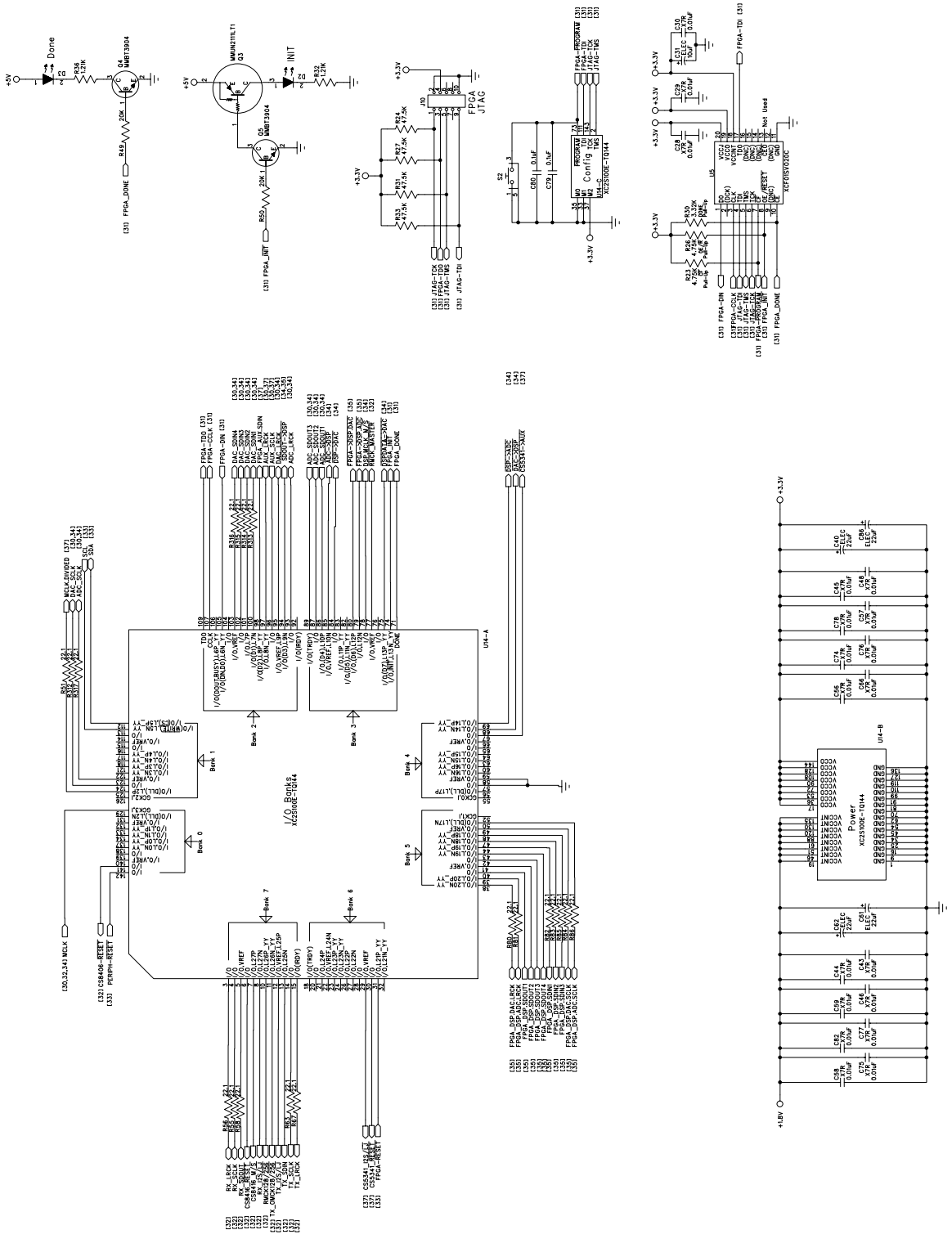

Figure 10. FPGA

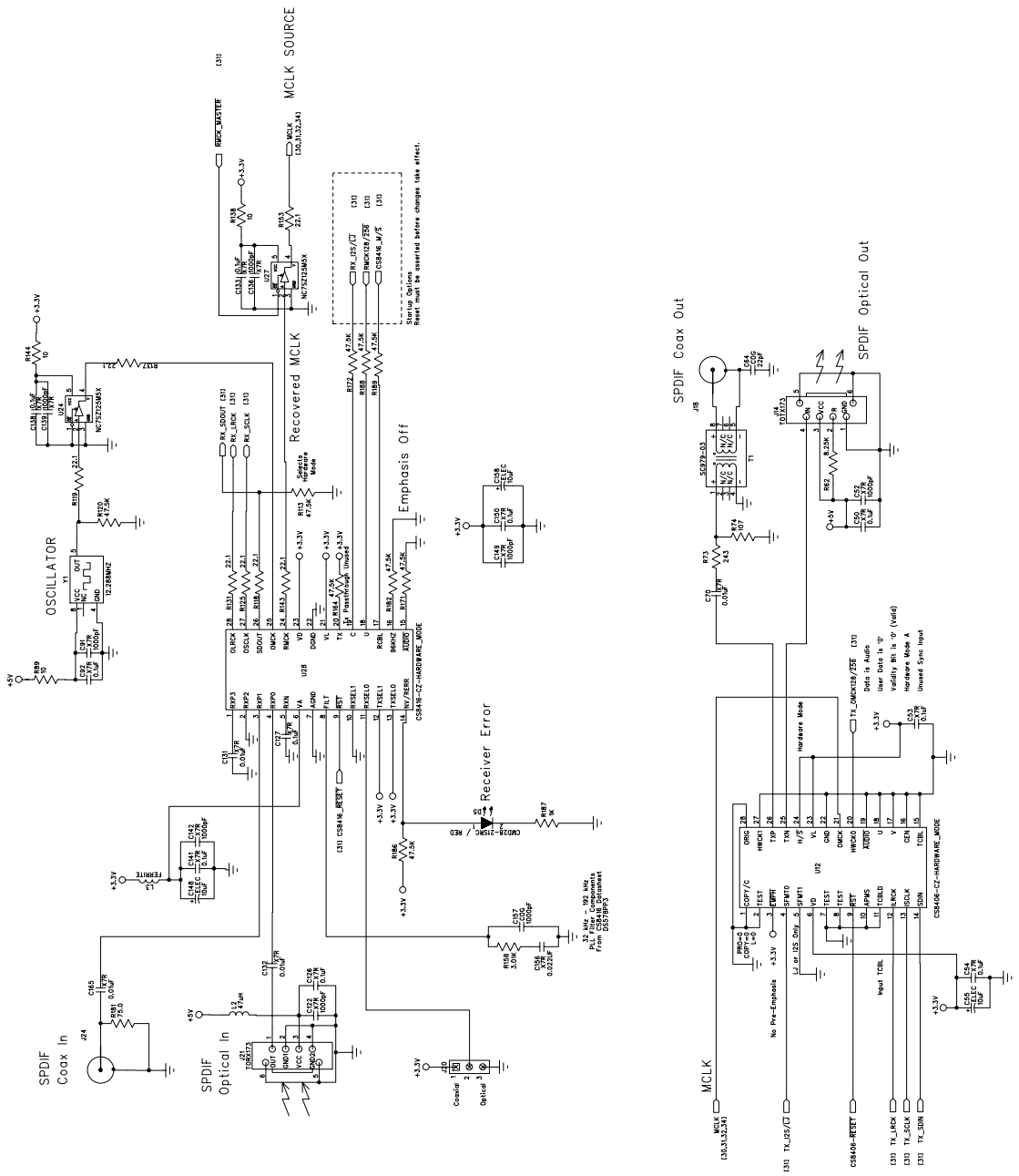

Figure 11. S/PDIF Input & Output

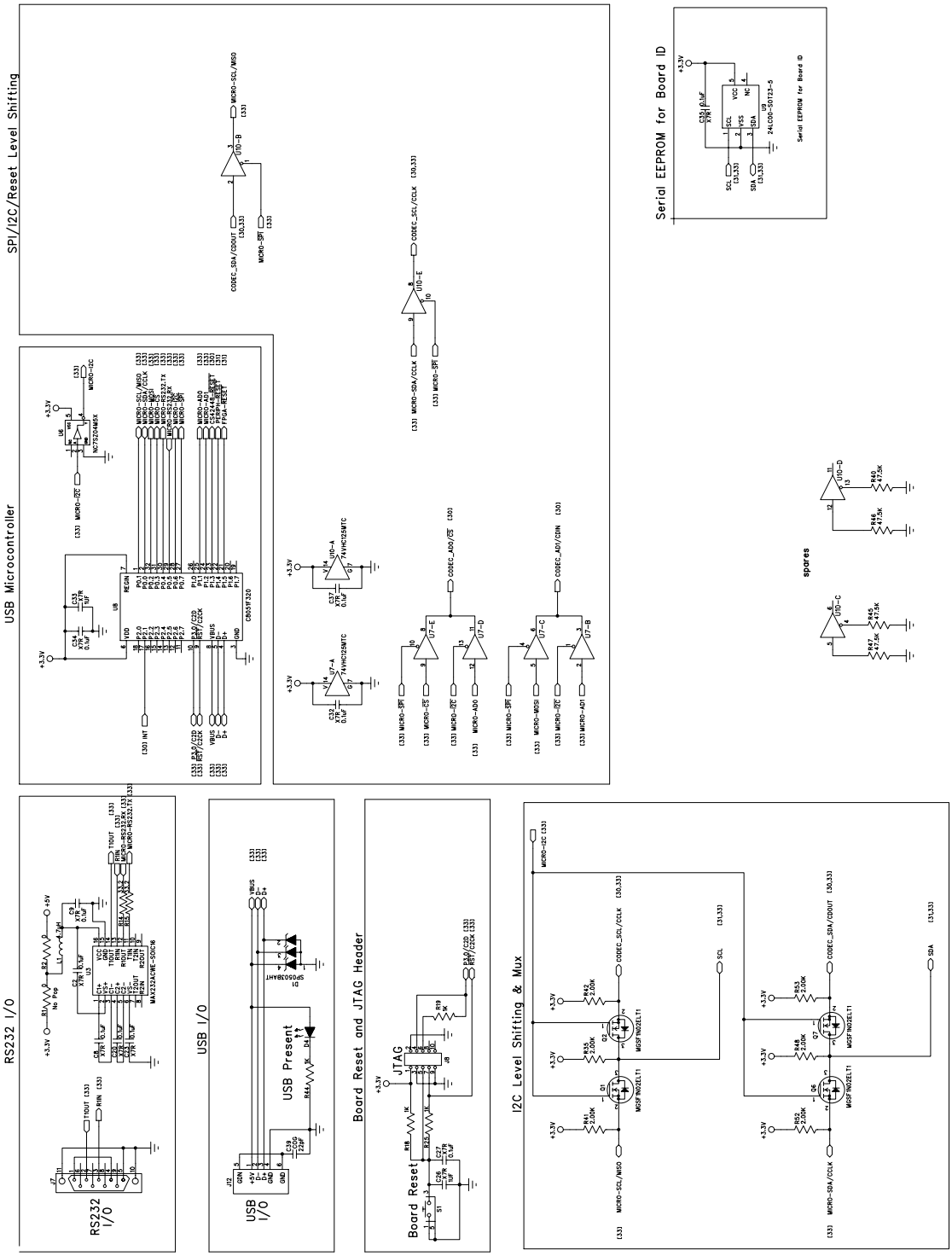

Figure 12. Control Port

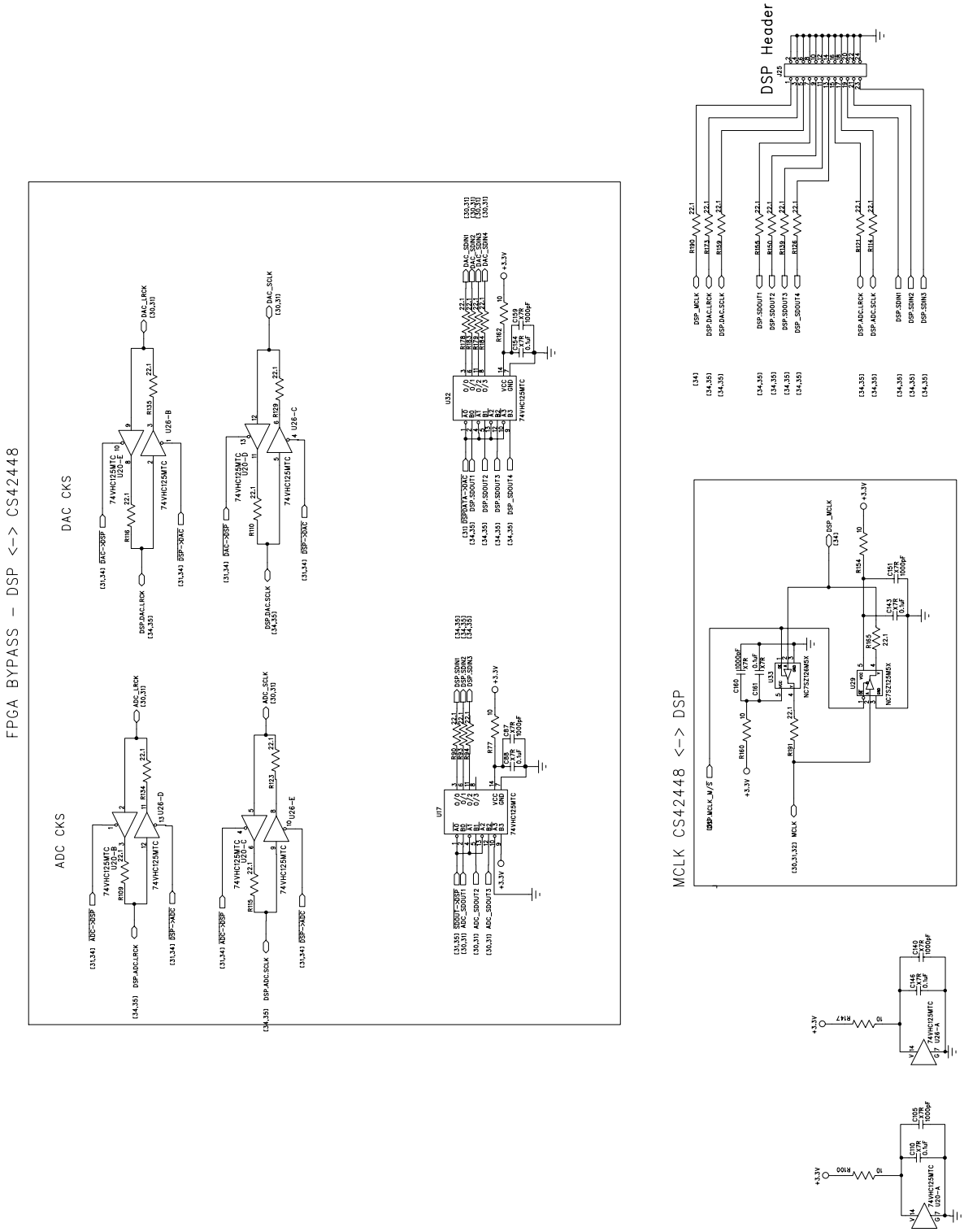

Figure 13. Buffers - FPGA Bypass

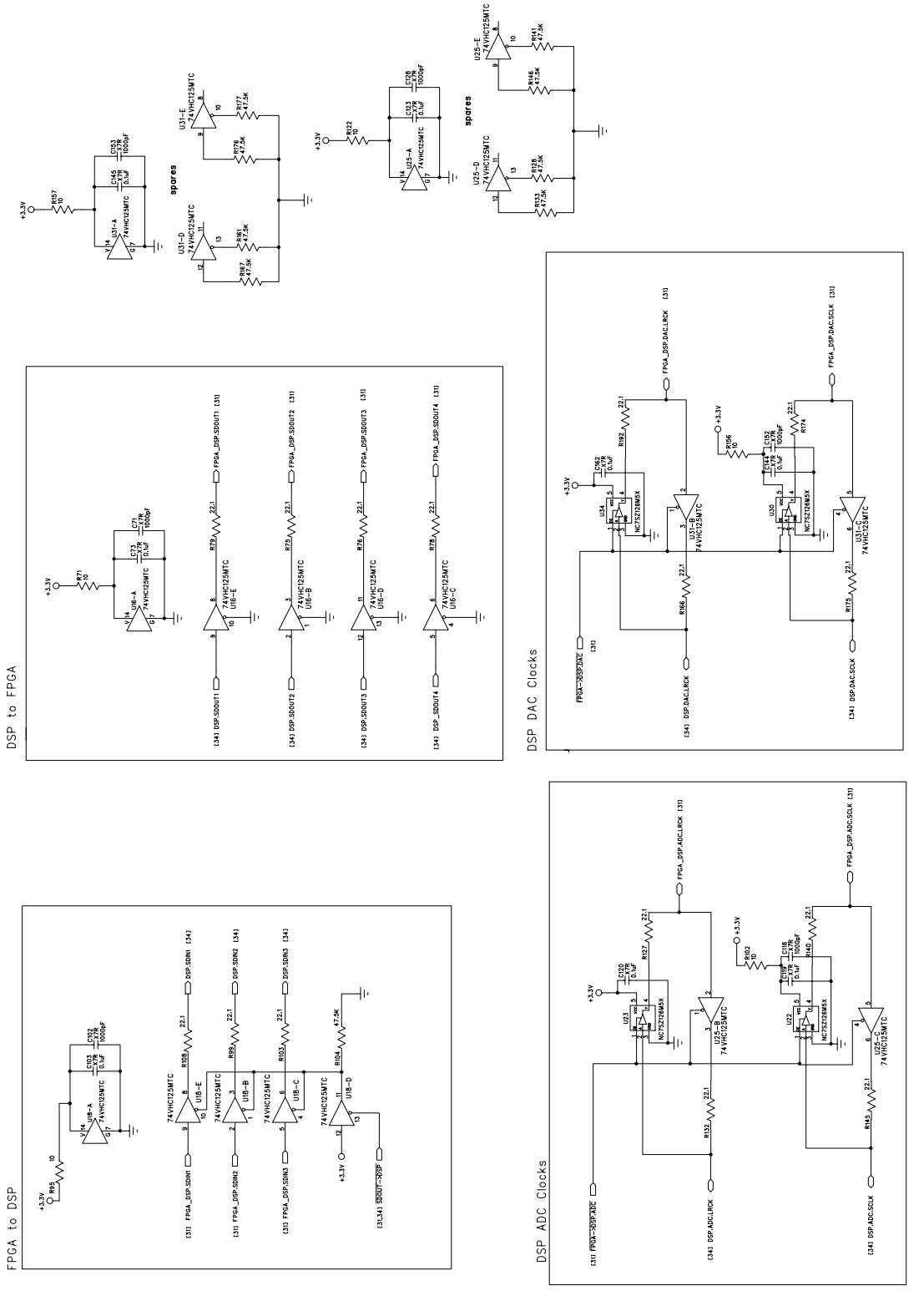

Figure 14. Buffers - DSP Routing

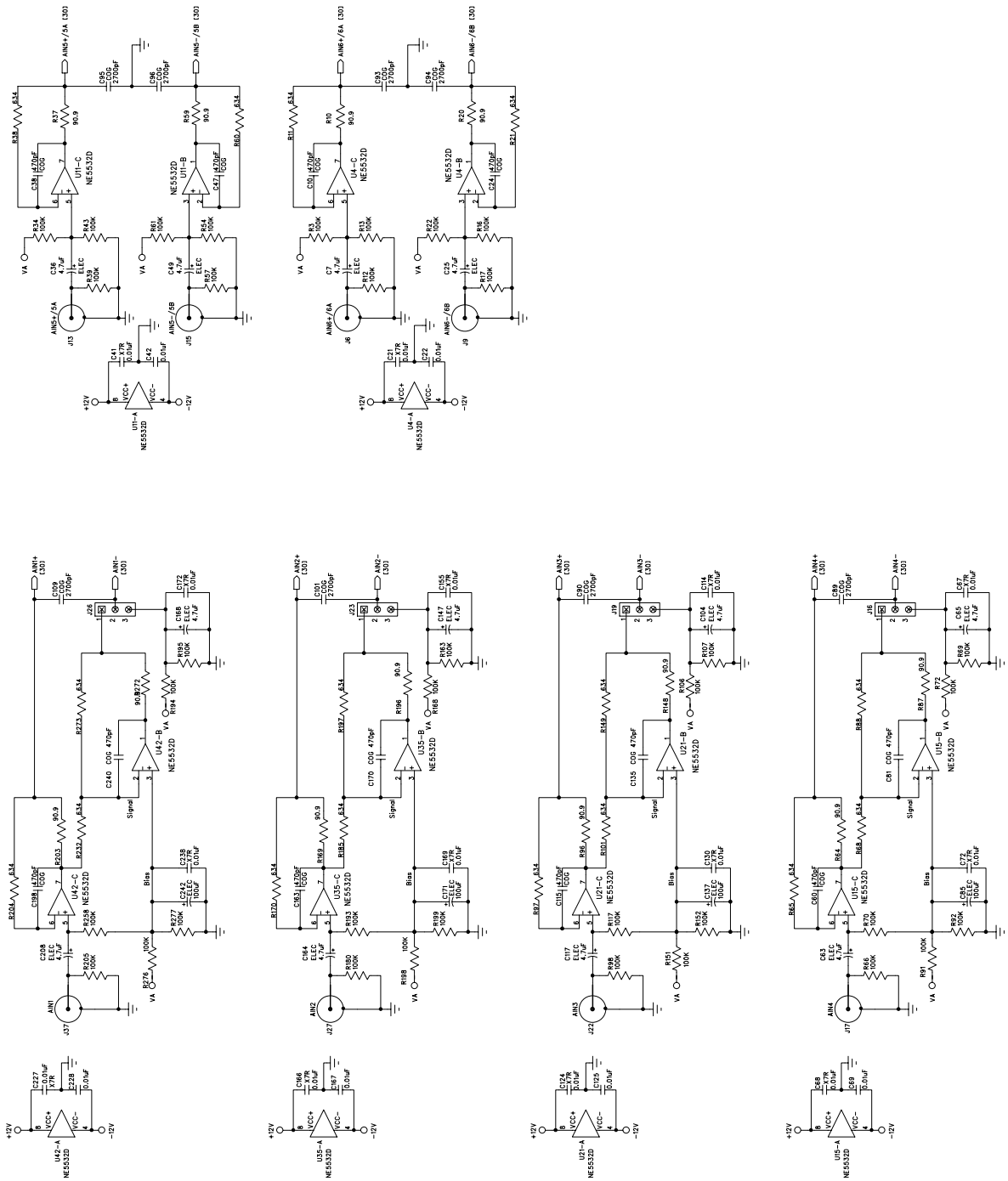

Figure 15. Analog Inputs

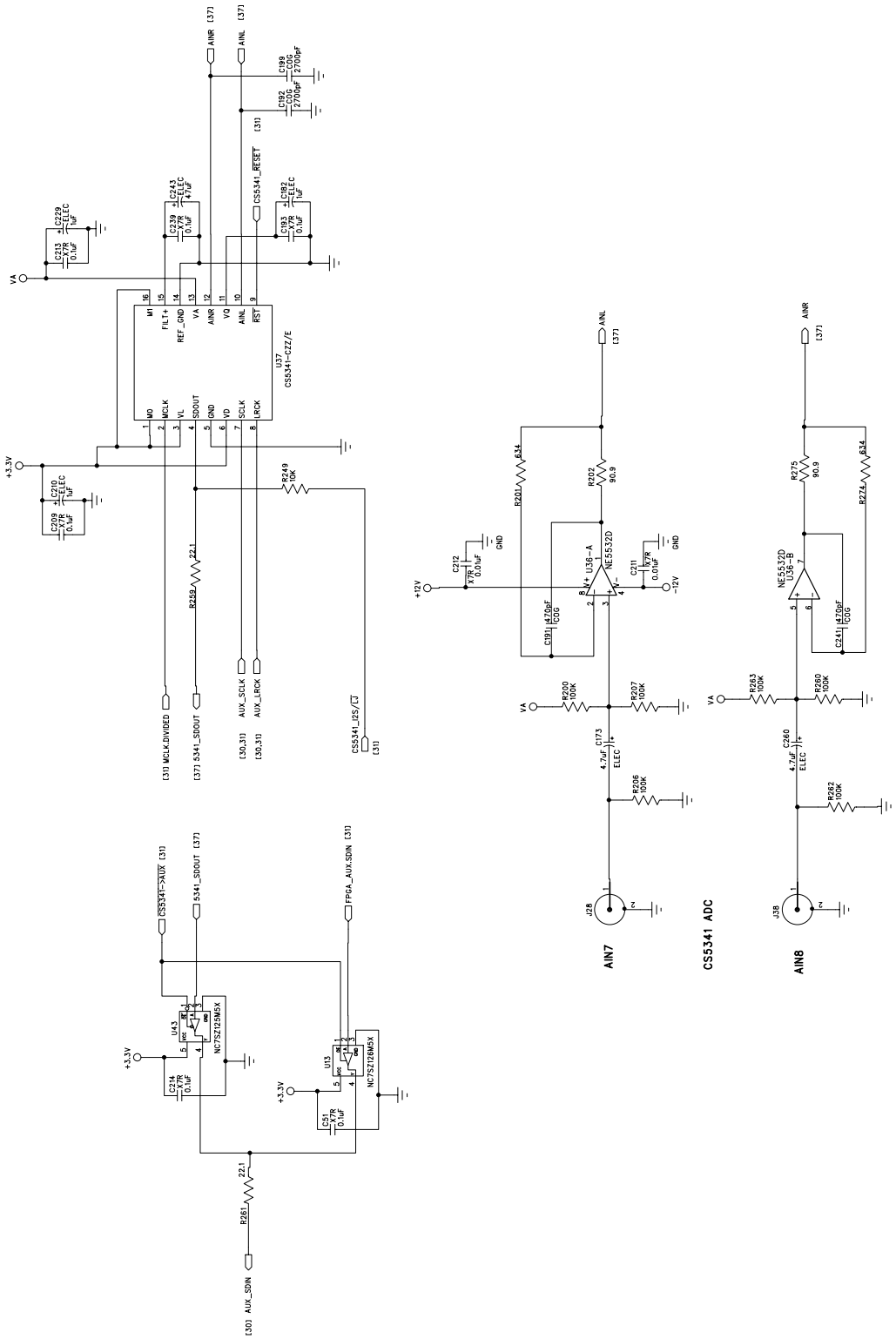

Figure 16. Auxiliary Input

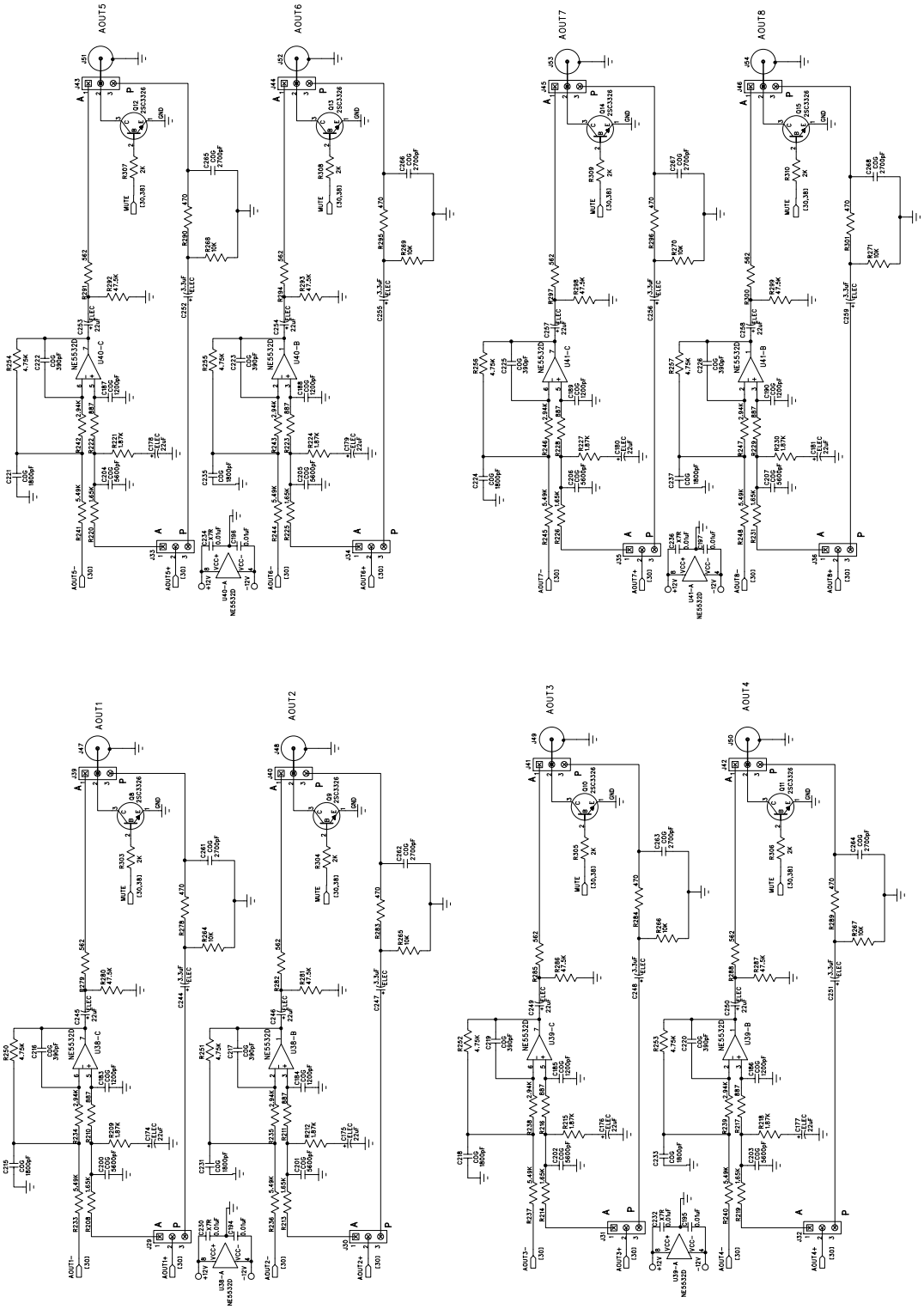

Figure 17. Analog Outputs

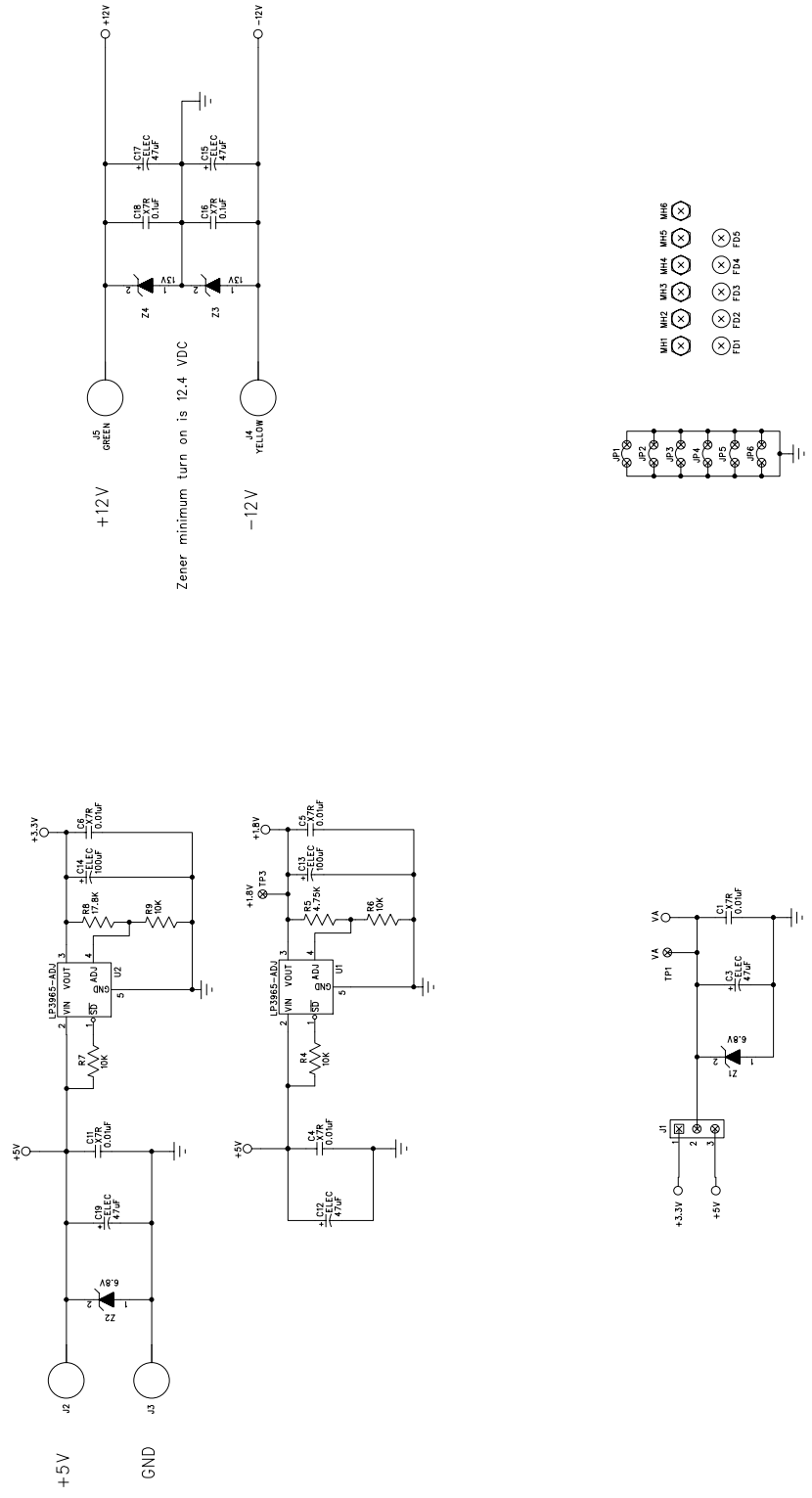

Figure 18. Power

9. CDB LAYOUT

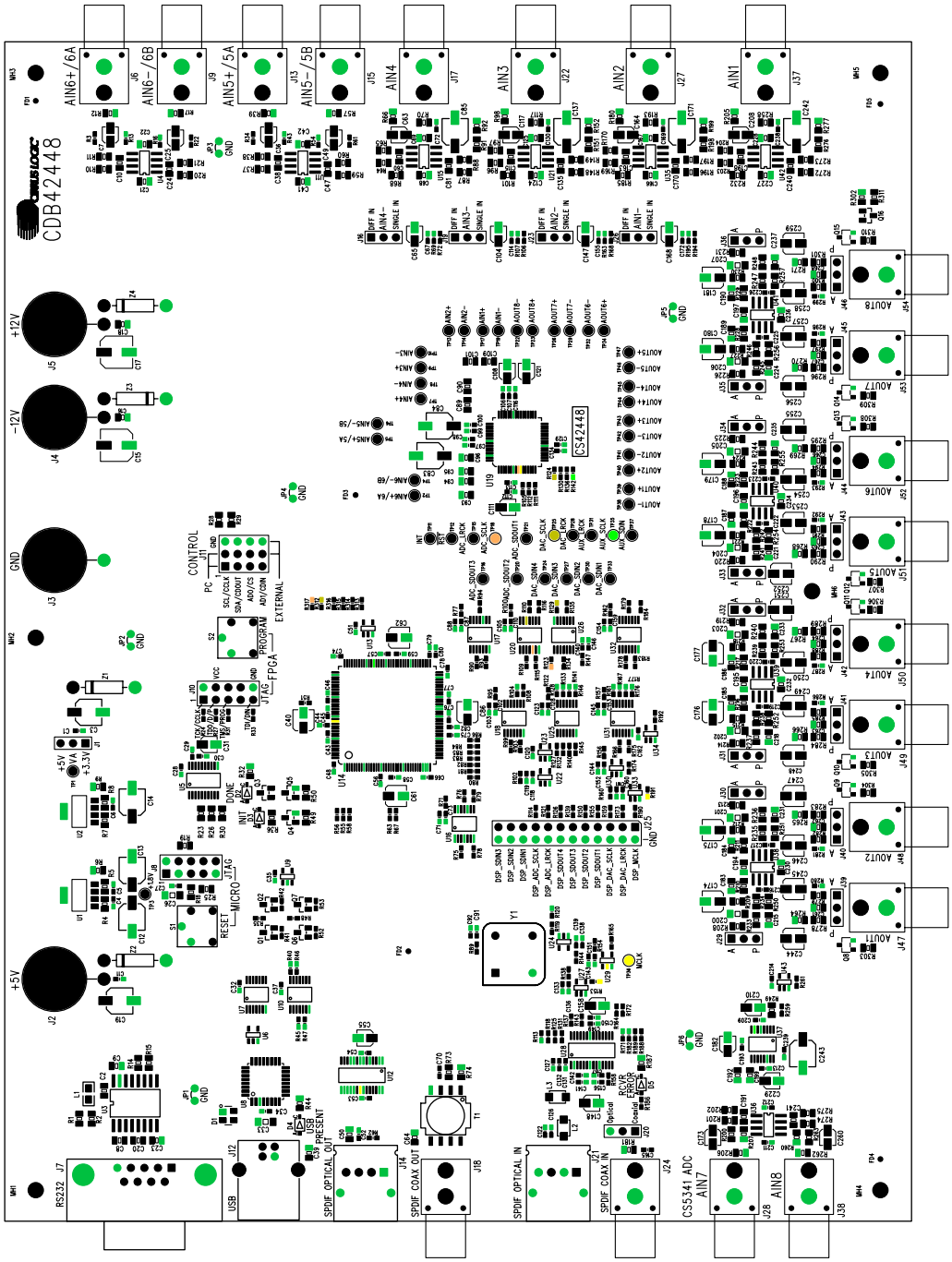

Figure 19. Silk Screen

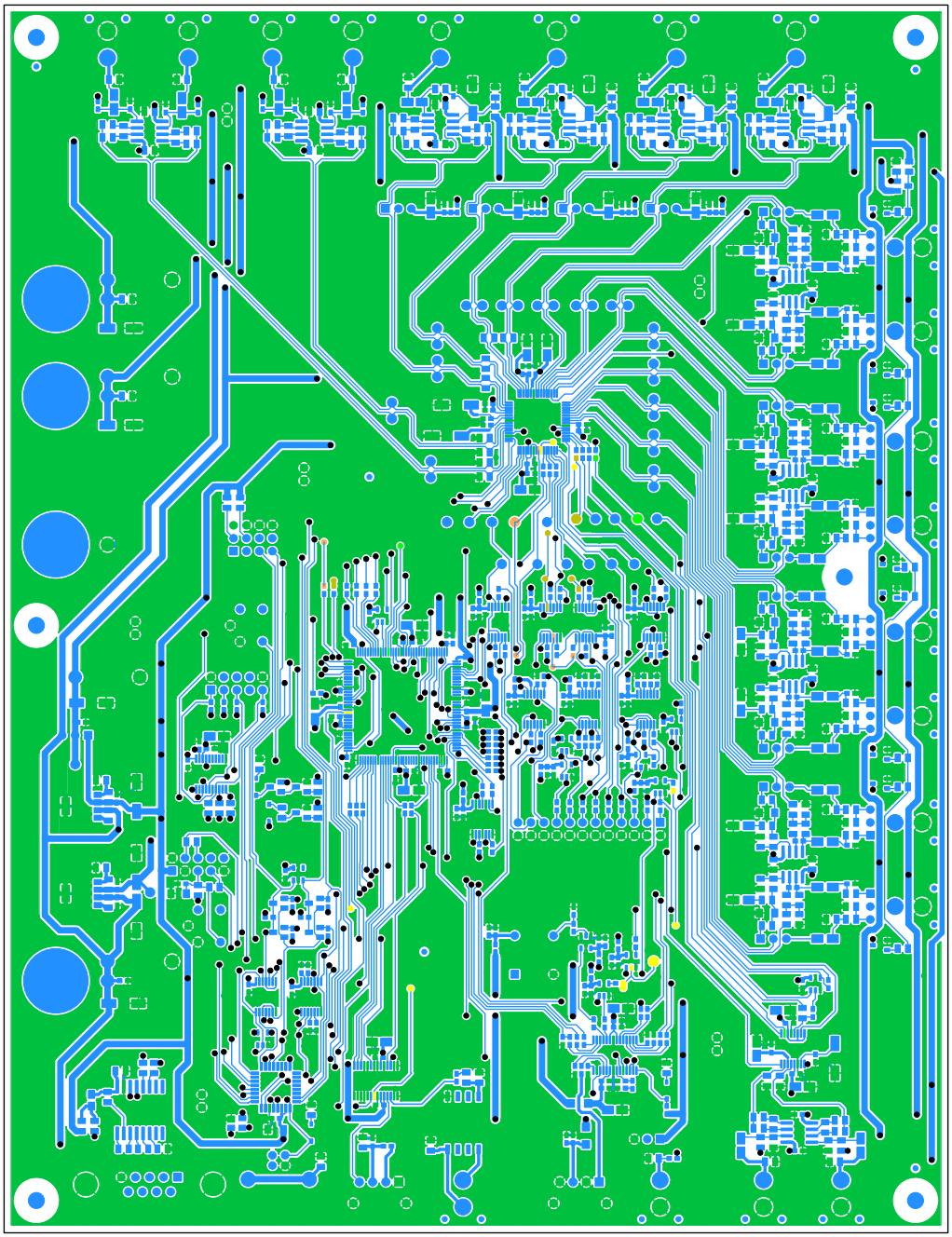

Figure 20. Topside Layer

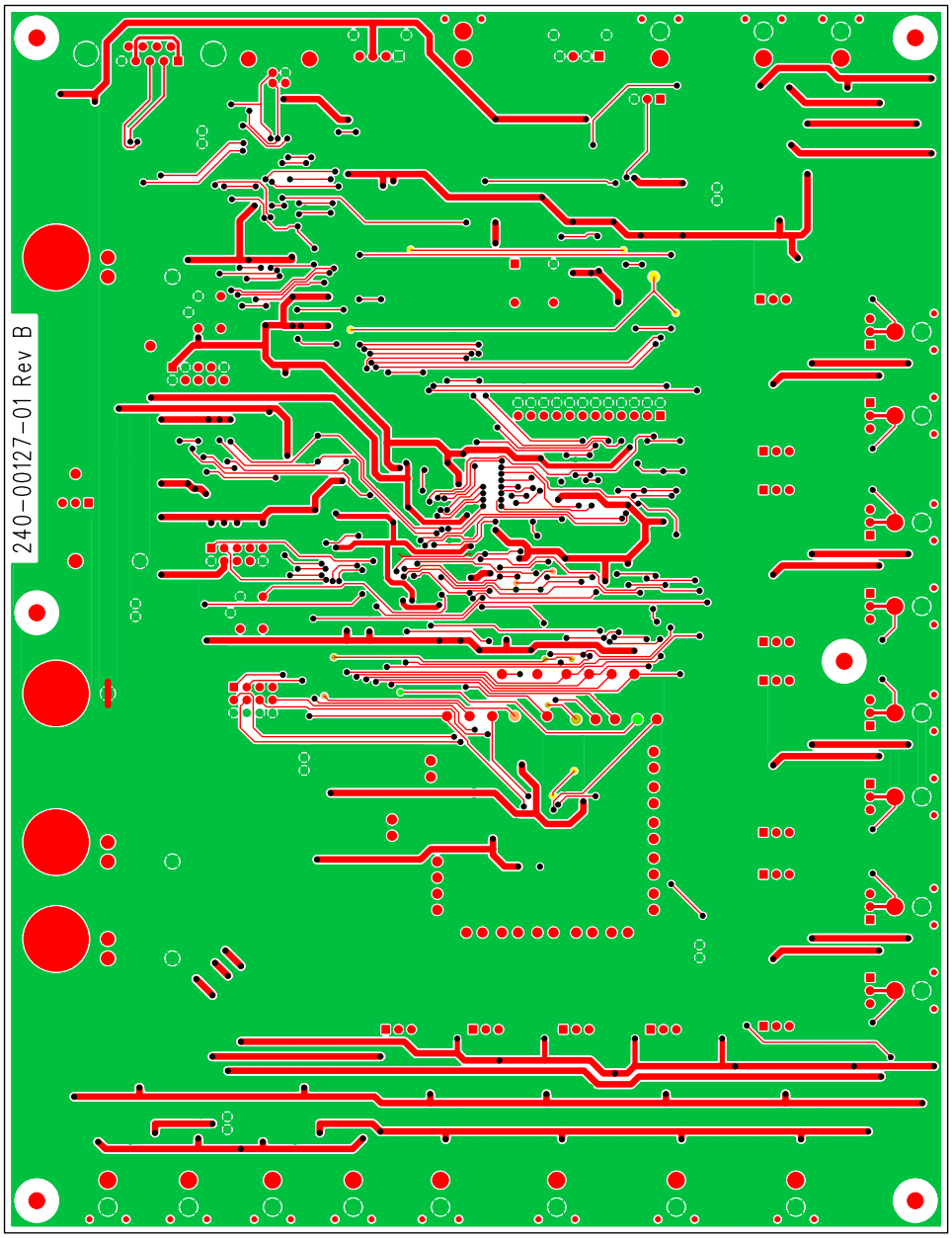

Figure 21. Bottom side Layer

10. REVISION HISTORY

Revision	Date	Changes
DB1	July 2004	Initial Release
DB2	OCT 2004	***Removed Bill of Materials*** ***Layer Changes***: *Corrected* silk screen lables for S1, J8, J11 on Figure 19 on page 41. *Changed* bottom layer lot number on Figure 21 on page 43.

Table 11. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**